(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号

特開平9－270659

(43)公開日　平成９年(1997)10月14日

(51)Int.Cl.[6]		識別記号	庁内整理番号	ＦＩ		技術表示箇所
Ｈ０３Ｈ	7/25			Ｈ０３Ｈ	7/25	
Ｈ０１Ｐ	1/15			Ｈ０１Ｐ	1/15	
	1/22				1/22	
Ｈ０３Ｇ	3/10			Ｈ０３Ｇ	3/10	Ａ
Ｈ０４Ｂ	1/44			Ｈ０４Ｂ	1/44	

審査請求　未請求　請求項の数10　ＯＬ　（全 15 頁）

(21)出願番号　特願平9－15766

(22)出願日　平成９年(1997)１月29日

(31)優先権主張番号　特願平8－14940

(32)優先日　平８(1996)１月31日

(33)優先権主張国　日本（ＪＰ）

(71)出願人　000005821
松下電器産業株式会社
大阪府門真市大字門真1006番地

(72)発明者　中塚　忠良
大阪府門真市大字門真1006番地　松下電器産業株式会社内

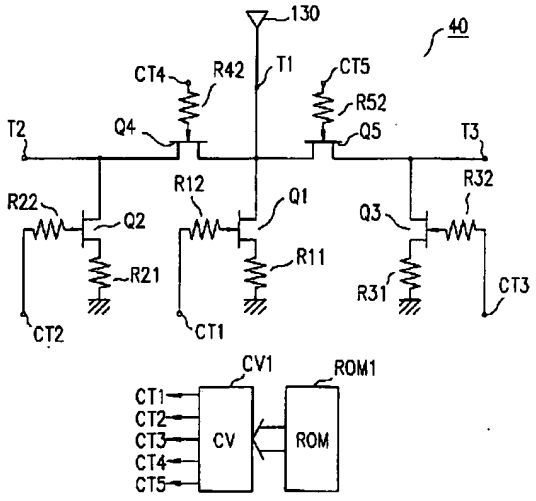
(74)代理人　弁理士　山本　秀策

(54)【発明の名称】　スイッチアッテネータ

(57)【要約】

【課題】　高周波機器に使用される高周波スイッチおよびアッテネータ回路において、機器の小型化、低コスト化を実現する。

【解決手段】　第１状態において、第１端子は、第２端子に接続され、第１端子は、第３端子から遮断され、第３端子は、グラウンドに接続され、第１端子からみたインピーダンスＺ１が第２端子からみたインピーダンスＺ２に実質的に等しい関係を維持しつつ、第１端子および第２端子の間の減衰量を変化させるように、スイッチアッテネータは電気的に制御可能であり、第２状態において、第１端子は、第３端子に接続され、第１端子は、第２端子から遮断され、第２端子は、グラウンドに接続され、第１端子からみたインピーダンスＺ１が第３端子からみたインピーダンスＺ３に実質的に等しい関係を維持しつつ、第１端子および第３端子の間の減衰量を変化させるように、スイッチアッテネータは電気的に制御可能である。



1

【特許請求の範囲】

【請求項１】　アンテナに接続される第１端子と、送信機に接続される第２端子と、受信機に接続される第３端子とを備え、第１状態および第２状態を切り替えるスイッチアッテネータであって、

該第１状態において、

該第１端子は、該第２端子に接続され、

該第１端子は、該第３端子から遮断され、

該第３端子は、グラウンドに接続され、

該第１端子からみたインピーダンスＺ１が該第２端子からみたインピーダンスＺ２に実質的に等しい関係を維持しつつ、該第１端子および該第２端子の間の減衰量を変化させるように、該スイッチアッテネータは電気的に制御可能であり、

該第２状態において、

該第１端子は、該第３端子に接続され、

該第１端子は、該第２端子から遮断され、

該第２端子は、グラウンドに接続され、

該第１端子からみたインピーダンスＺ１が該第３端子からみたインピーダンスＺ３に実質的に等しい関係を維持しつつ、該第１端子および該第３端子の間の減衰量を変化させるように、該スイッチアッテネータは電気的に制御可能であるスイッチアッテネータ。

【請求項２】　第１トランジスタが、前記第１端子とグラウンドとの間に設けられ、

第２トランジスタが、前記第２端子とグラウンドとの間に設けられ、

第３トランジスタが、前記第３端子とグラウンドとの間に設けられ、

第４トランジスタが、該第１端子と該第２端子との間に設けられ、

第５トランジスタが、該第１端子と該第３端子との間に設けられており、

前記第１状態において、

該第３トランジスタは、オン状態であり、

該第５トランジスタは、オフ状態であり、

前記第２状態において、

該第３トランジスタは、オン状態であり、

該第５トランジスタは、オフ状態である、請求項１に記載のスイッチアッテネータ。

【請求項３】　前記インピーダンスＺ１は、０．５×ＺＡ～２．０×ＺＡの範囲に実質的に含まれ、

前記インピーダンスＺ２は、０．５×ＺＴ～２．０×ＺＴの範囲に実質的に含まれ、

前記インピーダンスＺ３は、０．５×ＺＲ～２．０×ＺＲの範囲に実質的に含まれ、

ここでＺＡ、ＺＴおよびＺＲは、それぞれ前記アンテナ、前記送信機および前記受信機のインピーダンスを表す請求項１に記載のスイッチアッテネータ。

【請求項４】　前記第１トランジスタ、前記第２トランジスタ、前記第３トランジスタ、前記第４トランジスタおよび前記第５トランジスタのそれぞれは、ドレインと、ソースと、２つのゲートとを有するデュアルゲート電界効果トランジスタであり、該２つのゲートの一方のゲートは、該ドレインに接続されており、該２つのゲートの他方のゲートは、該ソースに接続されており、

該２つのゲートは、それぞれ抵抗を介して電気的な制御のための電圧を受け取る請求項３に記載のスイッチアッテネータ。

【請求項５】　第１アンテナに接続される第１端子と、送信機に接続される第２端子と、受信機に接続される第３端子と、第２アンテナに接続される第４端子とを備え、第１状態、第２状態、第３状態および第４状態を切り替えるスイッチアッテネータであって、

該第１状態においては、

該第１端子は、該第２端子に接続され、かつ該第３端子から遮断され、

該第３端子は、グラウンドに接続され、

該第４端子は、該第１端子、該第２端子、該第３端子および該グラウンドから遮断され、

該第１端子からみたインピーダンスＺ１が該第２端子からみたインピーダンスＺ２に実質的に等しい関係を維持しつつ、該第１端子および該第２端子の間の減衰量を変化させるように、該スイッチアッテネータは電気的に制御可能であり、

該第２状態においては、

該第１端子は、該第３端子に接続され、かつ該第２端子から遮断され、

該第２端子は、グラウンドに接続され、

該第４端子は、該第１端子、該第２端子、該第３端子および該グラウンドから遮断され、

該第１端子からみたインピーダンスＺ１が該第３端子からみたインピーダンスＺ３に実質的に等しい関係を維持しつつ、該第１端子および該第３端子の間の減衰量を変化させるように、該スイッチアッテネータは電気的に制御可能であり、

該第３状態においては、

該第４端子は、該第２端子に接続され、かつ該第３端子から遮断され、

該第３端子は、グラウンドに接続され、

該第１端子は、該第２端子、該第３端子、該第４端子および該グラウンドから遮断され、

該第４端子からみたインピーダンスＺ４が該第２端子からみたインピーダンスＺ２に実質的に等しい関係を維持しつつ、該第４端子および該第２端子の間の減衰量を変化させるように、該スイッチアッテネータは電気的に制御可能であり、

該第４状態においては、

該第４端子は、該第３端子に接続され、かつ該第２端子から遮断され、

該第２端子は、グラウンドに接続され、
該第１端子は、該第２端子、該第３端子、該第４端子および該グラウンドから遮断され、
該第４端子からみたインピーダンスＺ４が該第３端子からみたインピーダンスＺ３に実質的に等しい関係を維持しつつ、該第４端子および該第３端子の間の減衰量を変化させるように、該スイッチアッテネータは電気的に制御可能であるスイッチアッテネータ。
【請求項６】　第１トランジスタが、前記第１端子とグラウンドとの間に設けられ、
第２トランジスタが、前記第２端子とグラウンドとの間に設けられ、
第３トランジスタが、前記第３端子とグラウンドとの間に設けられ、
第４トランジスタが、該第１端子と該第２端子との間に設けられ、
第５トランジスタが、該第１端子と該第３端子との間に設けられ、
第６トランジスタが、前記第４端子とグラウンドとの間に設けられ、
第７トランジスタが、該第２端子と該第４端子との間に設けられ、
第８トランジスタが、該第３端子と該第４端子との間に設けられ、
前記第１状態において、
該第３トランジスタは、オン状態であり、
該第５トランジスタ、該第６トランジスタ、該第７トランジスタおよび該第８トランジスタは、オフ状態であり、
前記第２状態において、
該第２トランジスタは、オン状態であり、
該第４トランジスタ、該第６トランジスタ、該第７トランジスタおよび該第８トランジスタは、オフ状態であり、
前記第３状態において、
該第３トランジスタは、オン状態であり、
該第１トランジスタ、該第４トランジスタ、該第５トランジスタおよび該第８トランジスタは、オフ状態であり、
前記第４状態において、
該第２トランジスタは、オン状態であり、
該第１トランジスタ、該第４トランジスタ、該第５トランジスタおよび該第７トランジスタは、オフ状態である、請求項５に記載のスイッチアッテネータ。
【請求項７】　前記インピーダンスＺ１およびＺ４は、０．５×ＺＡ～２．０×ＺＡの範囲に実質的に含まれ、
前記インピーダンスＺ２は、０．５×ＺＴ～２．０×ＺＴの範囲に実質的に含まれ、
前記インピーダンスＺ３は、０．５×ＺＲ～２．０×ＺＲの範囲に実質的に含まれ、

ここでＺＡ、ＺＴおよびＺＲは、それぞれ前記アンテナ、前記送信機および前記受信機のインピーダンスを表す請求項５に記載のスイッチアッテネータ。
【請求項８】　半導体基板上に集積化されて形成されている請求項１から請求項７のいずれかに記載のスイッチアッテネータ。
【請求項９】　電力増幅器をさらに備えており、該電力増幅器は、前記半導体基板上に集積化されて形成されている請求項８に記載のスイッチアッテネータ。
【請求項１０】　低雑音増幅器をさらに備えており、該低雑音増幅器は、前記半導体基板上に集積化されて形成されている請求項９に記載のスイッチアッテネータ。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は高周波送受信回路に使用される高周波スイッチおよび高周波アッテネータを含むスイッチアッテネータに関する。また本発明は、このスイッチアッテネータを実現する半導体デバイスと、この半導体デバイスを用いた高周波機器とにも関する。
【０００２】
【従来の技術】図１は、従来の技術による送受信回路の高周波（以下「ＲＦ」とする）部１０を示すブロック図である。送受信回路のＲＦ部１０は、ＲＦスイッチ１２０を備えており、これにより送信および受信を選択的におこなう。送信時には、変調信号入力端子（ＭＯＤ　ｉｎ）１１０において入力された信号は、周波数変換器（以下「ミキサ」とする）１１２、可変利得増幅器（以下「ＡＧＣアンプ」とする）１１４、電力増幅器（ＰＡ）１１６、ＲＦスイッチ（ＲＦ　ＳＷ）１２０および周波数フィルタ１２２を通ってアンテナ１３０から空間へ輻射される。
【０００３】逆に受信時には、アンテナ１３０において受け取られた信号は、周波数フィルタ１２２、ＲＦスイッチ１２０、減衰器１５０、低雑音増幅器（ＬＮＡ）１５２およびミキサ１５４を通って中間周波（以下「ＩＦ」とする）信号出力端子（ＩＦ　ｏｕｔ）１５６から出力される。
【０００４】送受信いずれの場合も、フェーズロックドループ（以下「ＰＬＬ」とする）１７０および発振器１７２は、所望の周波数をもつ局部発振信号を発生し、信号分配器（ＤＩＶ）１７４に出力する。ミキサ１１２は、変調信号および局部発振信号を混合することによって、ＲＦ信号を生成し、ＡＧＣアンプ１１４に出力する。ミキサ１５４は、ＲＦ信号および局部発振信号を混合することによって、ＩＦ信号を生成し、ＩＦ信号出力端子１５６に出力する。
【０００５】図１のＲＦ部１０の動作を以下に説明する。ＲＦ部１０は、例えば携帯電話の端末機に代表される移動体通信機の一部である。移動体通信機においては、機器構成の簡略化のために、比較的、大きな体積を

要するアンテナ１３０（ここでは周波数フィルタ１２２も含めて考える）は、ほとんどの場合において送信回路および受信回路の双方のために使用される。アンテナ部を送受信で共用するために送信時においては、アンテナ１３０は、電力増幅器１１６に電気的に結合され、かつ低雑音増幅器１５２から電気的に分離される。逆に受信時においては、アンテナ１３０は、電力増幅器１１６から電気的に分離され、かつ低雑音増幅器１５２に電気的に結合される。このような送受信のための切替をおこなうために、通常、半導体素子化されたＲＦスイッチ１２０が採用される。従来技術によるＲＦスイッチ１２０は、スイッチング素子としてトランジスタを用いており、トランジスタがオン状態およびオフ状態のいずれかの状態をとるように電気的に制御している。

【０００６】また移動体通信における端末機（例えば携帯電話のハンドセットそのもの）は、最寄りの基地局にＲＦ信号を送信し、基地局からＲＦ信号を受信することによって通信をおこなう。基地局において受信される電力をほぼ一定に維持するために、端末機と基地局との距離に応じて、端末機から送信される電力を微妙に制御する必要がある。反対に端末機のＩＦ信号出力端子１５６において出力される電力をほぼ一定に維持するためには、低雑音増幅器１５２に入力されるＲＦ電力を制御する必要がある。これらの要求を満たすため端末機のＲＦ部１０は一般に、送信のためのＡＧＣアンプ１１４と、受信のためのアッテネータ１５０とを備えている。

【０００７】図２は、従来の技術によるスイッチ２０の回路図である。図２において、スイッチ２０は、電界効果トランジスタ（以下「ＦＥＴ」とする）２００～２０３、インピーダンス調整用抵抗器２１０および２１１、ゲートバイアス抵抗器２２０～２２３、アンテナ端子２３０、送信電力入力端子２３１、受信電力出力端子２３２、第１制御端子２４５および第２制御端子２４６を備えている。

【０００８】図２のスイッチの動作を説明する。送信時には、ＦＥＴ２０１および２０２の閾値の絶対値より大きい負の電圧を第２制御端子２４６に印加することによって、ＦＥＴ２０１および２０２をオフ状態にし、かつゼロまたは正の電圧を第１制御端子２４５に印加し、ＦＥＴ２００および２０３をオン状態にする。これにより、送信電力は、端子２３１、ＦＥＴ２００およびアンテナ端子２３０を通って、アンテナ２５０に出力される。

【０００９】逆に受信時には、ＦＥＴ２００および２０３の閾値の絶対値より大きい負の電圧を第１制御端子２４５に印加することによって、ＦＥＴ２００および２０３をオフ状態にし、かつゼロまたは正の電圧を第２制御端子２４６に印加してＦＥＴ２０１および２０２をオン状態にする。これにより、受信電力は、アンテナ２５０、端子２３０およびＦＥＴ２０１を通って、端子２３２に出力される。

【００１０】

【発明が解決しようとする課題】携帯電話の移動端末機器においては、携帯性を高めるため機器を小型・軽量化するとともに、低コスト化することが重要である。これを実現するために現在、ＲＦ部における回路の小型化および低コスト化が強く求められている。ところが上述のいずれの従来技術においても、送受信回路は、スイッチ、ＡＧＣアンプおよびアッテネータを別個に備えることが必要であった。その結果、従来の技術による送受信回路は、機器のサイズおよびコストの増大が不可避であるという課題を有していた。

【００１１】本発明は、上記課題を解決するためになされたものであり、その目的とするところは、高周波送受信回路に用いられる小型・軽量および低コストな、スイッチおよびアッテネータとして機能する装置を提供することにある。

【００１２】

【課題を解決するための手段】本発明によるスイッチアッテネータは、アンテナに接続される第１端子と、送信機に接続される第２端子と、受信機に接続される第３端子とを備え、第１状態および第２状態を切り替えるスイッチアッテネータであって、該第１状態において、該第１端子は、該第２端子に接続され、該第１端子は、該第３端子から遮断され、該第３端子は、グラウンドに接続され、該第１端子からみたインピーダンスＺ１が該第２端子からみたインピーダンスＺ２に実質的に等しい関係を維持しつつ、該第１端子および該第２端子の間の減衰量を変化させるように、該スイッチアッテネータは電気的に制御可能であり、該第２状態において、該第１端子は、該第３端子に接続され、該第１端子は、該第２端子から遮断され、該第２端子は、グラウンドに接続され、該第１端子からみたインピーダンスＺ１が該第３端子からみたインピーダンスＺ３に実質的に等しい関係を維持しつつ、該第１端子および該第３端子の間の減衰量を変化させるように、該スイッチアッテネータは電気的に制御可能であり、そのことにより上記目的が達成される。

【００１３】ある実施形態では、第１トランジスタが、前記第１端子とグラウンドとの間に設けられ、第２トランジスタが、前記第２端子とグラウンドとの間に設けられ、第３トランジスタが、前記第３端子とグラウンドとの間に設けられ、第４トランジスタが、該第１端子と該第２端子との間に設けられ、第５トランジスタが、該第１端子と該第３端子との間に設けられており、前記第１状態において、該第３トランジスタは、オン状態であり、該第５トランジスタは、オフ状態であり、前記第２状態において、該第３トランジスタは、オン状態であり、該第５トランジスタは、オフ状態である。

【００１４】ある実施形態では、前記インピーダンスＺ１は、０．５×ＺＡ～２．０×ＺＡの範囲に実質的に含

まれ、前記インピーダンスＺ２は、０．５×ＺＴ～２．０×ＺＴの範囲に実質的に含まれ、前記インピーダンスＺ３は、０．５×ＺＲ～２．０×ＺＲの範囲に実質的に含まれ、ここでＺＡ、ＺＴおよびＺＲは、それぞれ前記アンテナ、前記送信機および前記受信機のインピーダンスを表す。

【００１５】ある実施形態では、前記第１トランジスタ、前記第２トランジスタ、前記第３トランジスタ、前記第４トランジスタおよび前記第５トランジスタのそれぞれは、ドレインと、ソースと、２つのゲートとを有するデュアルゲート電界効果トランジスタであり、該２つのゲートの一方のゲートは、該ドレインに接続されており、該２つのゲートの他方のゲートは、該ソースに接続されており、該２つのゲートは、それぞれ抵抗を介して電気的な制御のための電圧を受け取る。

【００１６】本発明によるスイッチアッテネータは、第１アンテナに接続される第１端子と、送信機に接続される第２端子と、受信機に接続される第３端子と、第２アンテナに接続される第４端子とを備え、第１状態、第２状態、第３状態および第４状態を切り替えるスイッチアッテネータであって、該第１状態においては、該第１端子は、該第２端子に接続され、かつ該第３端子から遮断され、該第３端子は、グラウンドに接続され、該第４端子は、該第１端子、該第２端子、該第３端子および該グラウンドから遮断され、該第１端子からみたインピーダンスＺ１が該第２端子からみたインピーダンスＺ２に実質的に等しい関係を維持しつつ、該第１端子および該第２端子の間の減衰量を変化させるように、該スイッチアッテネータは電気的に制御可能であり、該第２状態においては、該第１端子は、該第３端子に接続され、かつ該第２端子から遮断され、該第２端子は、グラウンドに接続され、該第４端子は、該第１端子、該第２端子、該第３端子および該グラウンドから遮断され、該第１端子からみたインピーダンスＺ１が該第３端子からみたインピーダンスＺ３に実質的に等しい関係を維持しつつ、該第１端子および該第３端子の間の減衰量を変化させるように、該スイッチアッテネータは電気的に制御可能であり、該第３状態においては、該第４端子は、該第２端子に接続され、かつ該第３端子から遮断され、該第３端子は、グラウンドに接続され、該第１端子は、該第２端子、該第３端子、該第４端子および該グラウンドから遮断され、該第４端子からみたインピーダンスＺ４が該第２端子からみたインピーダンスＺ２に実質的に等しい関係を維持しつつ、該第４端子および該第２端子の間の減衰量を変化させるように、該スイッチアッテネータは電気的に制御可能であり、該第４状態においては、該第４端子は、該第３端子に接続され、かつ該第２端子から遮断され、該第２端子は、グラウンドに接続され、該第１端子は、該第２端子、該第３端子、該第４端子および該グラウンドから遮断され、該第４端子からみたインピーダンスＺ４が該第３端子からみたインピーダンスＺ３に実質的に等しい関係を維持しつつ、該第４端子および該第３端子の間の減衰量を変化させるように、該スイッチアッテネータは電気的に制御可能であり、そのことにより上記目的が達成される。

【００１７】ある実施形態では、第１トランジスタが、前記第１端子とグラウンドとの間に設けられ、第２トランジスタが、前記第２端子とグラウンドとの間に設けられ、第３トランジスタが、前記第３端子とグラウンドとの間に設けられ、第４トランジスタが、該第１端子と該第２端子との間に設けられ、第５トランジスタが、該第１端子と該第３端子との間に設けられ、第６トランジスタが、前記第４端子とグラウンドとの間に設けられ、第７トランジスタが、該第２端子と該第４端子との間に設けられ、第８トランジスタが、該第３端子と該第４端子との間に設けられ、前記第１状態において、該第３トランジスタは、オン状態であり、該第５トランジスタ、該第６トランジスタ、該第７トランジスタおよび該第８トランジスタは、オフ状態であり、前記第２状態において、該第２トランジスタは、オン状態であり、該第４トランジスタ、該第６トランジスタ、該第７トランジスタおよび該第８トランジスタは、オフ状態であり、前記第３状態において、該第３トランジスタは、オン状態であり、該第１トランジスタ、該第４トランジスタ、該第５トランジスタおよび該第８トランジスタは、オフ状態であり、前記第４状態において、該第２トランジスタは、オン状態であり、該第１トランジスタ、該第４トランジスタ、該第５トランジスタおよび該第７トランジスタは、オフ状態である。

【００１８】ある実施形態では、前記インピーダンスＺ１およびＺ４は、０．５×ＺＡ～２．０×ＺＡの範囲に実質的に含まれ、前記インピーダンスＺ２は、０．５×ＺＴ～２．０×ＺＴの範囲に実質的に含まれ、前記インピーダンスＺ３は、０．５×ＺＲ～２．０×ＺＲの範囲に実質的に含まれ、ここでＺＡ、ＺＴおよびＺＲは、それぞれ前記アンテナ、前記送信機および前記受信機のインピーダンスを表す。

【００１９】ある実施形態では、半導体基板上に集積化されて形成されている。

【００２０】ある実施形態では、電力増幅器をさらに備えており、該電力増幅器は、前記半導体基板上に集積化されて形成されている。

【００２１】ある実施形態では、低雑音増幅器をさらに備えており、該低雑音増幅器は、前記半導体基板上に集積化されて形成されている。

【００２２】

【発明の実施の形態】以下、本発明の実施の形態を図面を参照しながら説明する。同じ参照符号は、同じ構成要素を表す。

【００２３】本明細書における「スイッチアッテネー

タ」は、後述するようにアンテナ用ＲＦスイッチとＲＦアッテネータとの機能を併せもつ装置をいう。また「ノード」は、装置外部への接続のための端子を必ずしも必要としない。

【００２４】（実施の形態１）図３は、本発明のスイッチアッテネータの第１の実施形態が用いられる携帯電話機のＲＦ部３０のブロック図である。本発明のスイッチアッテネータ４０は、送受信の状態に応じて、アンテナ１３０と、電力増幅器１１６または低雑音増幅器１５２とを電気的に結合する。より具体的には、スイッチアッテネータ４０は、送信時にはノードＴ１をノードＴ２に電気的に結合し、ノードＴ３をグラウンドに電気的に結合する。またスイッチアッテネータ４０は、受信時にはノードＴ１をノードＴ３に電気的に結合し、ノードＴ２をグラウンドに電気的に結合する。本明細書におけるグラウンドは、電源の負極が接続されており、直流（以下「ＤＣ」とする）信号およびＲＦ信号の双方について共通電位を提供するとともに、高周波的にシールドされた筐体などにも接続されている。ＲＦ部３０における送受信時の信号の流れは、図１で説明したのと同様である。

【００２５】本発明によるスイッチアッテネータ４０は、後述するように、スイッチおよびアッテネータの機能を併せもつので、図１のＡＧＣアンプ１１４およびアッテネータ１５０をなくすことができるという大きな効果を有する。またスイッチアッテネータ４０を一体化された半導体デバイスとして製造すれば、サイズおよびコストの大幅な削減が可能となりより好ましい。なお図３のそれぞれのブロックを接続する伝送線路は、すべて５０Ωの特性インピーダンスを有する。またここではＲＦ部３０は、携帯電話機の一部として用いられているが、これには限定されない。ＲＦ部３０は、ＲＦ信号を送受信する装置に広く利用することができ、またスイッチアッテネータ４０は、ＲＦ信号を切り替えるとともに、減衰させる装置として広く利用できる。

【００２６】図３において、制御電圧発生器ＣＶ１は、スイッチアッテネータ４０に含まれるＦＥＴの状態を後で説明する表１～表４のように設定するための制御電圧をリードオンリーメモリＲＯＭ１に格納されたデータに基づいて発生し、それぞれのＦＥＴに供給する。リードオンリーメモリＲＯＭ１は、表１～表４の状態に対応するＦＥＴの制御電圧を発生するためのデータを格納する。

【００２７】図４は、本発明によるスイッチアッテネータの第１の実施形態の回路図である。スイッチアッテネータ４０は、ノードＴ１、Ｔ２およびＴ３を備えており、それぞれアンテナ１３０、電力増幅器１１６および低雑音増幅器１５２に接続されている。制御電圧発生器ＣＶ１は、リードオンリーメモリＲＯＭ１に格納されたデータに基づいてＦＥＴを制御する電圧を発生し、ノードＣＴ１～ＣＴ５に出力する。

【００２８】ＦＥＴ　Ｑ１は、ノードＴ１をあるインピーダンスでグラウンドに接続する。ノードＣＴ１において受け取られた制御電圧は、抵抗Ｒ１２を介してＦＥＴ　Ｑ１のゲートに加えられ、ＦＥＴ　Ｑ１のこの所定のインピーダンスを変化させる。具体的には、ノードＣＴ１の制御電圧に応じて、ＦＥＴ　Ｑ１は、オン状態からオフ状態までの広い範囲のインピーダンスをとりうる。ＦＥＴ　Ｑ１のインピーダンスは、オン状態ではゼロであるとみなせる程度に低く、オフ状態では無限大であるとみなせる程度に高い。ＦＥＴ　Ｑ１はＮ型のディプレッション型であるので、ＦＥＴ　Ｑ１をオン状態にするためには、０［Ｖ］以上のゲート・ソース間電圧Ｖｇｓを与えればよく、逆にＦＥＴ　Ｑ１をオフ状態にするためには、閾値ＶＴＨ［Ｖ］（ＶＴＨ＜０）以下のゲート・ソース間電圧Ｖｇｓを与えればよい。ＦＥＴ　Ｑ１のゲート・ソース間電圧Ｖｇｓが、ＶＴＨ＜Ｖｇｓ＜０なる関係を満たすとき、本明細書においてはＦＥＴ　Ｑ１は、オン状態とオフ状態との「中間状態」であるとよぶことにする。ＦＥＴ　Ｑ１は、本実施の形態では、ショットキー接合ゲート型ＦＥＴ（以下「ＭＥＳＦＥＴ」とする）である。以上、ＦＥＴ　Ｑ１についての説明は、本明細書において、ＦＥＴ　Ｑ２～Ｑ４についてもあてはまる。

【００２９】ＦＥＴ　Ｑ１と同様に、ＦＥＴ　Ｑ２およびＱ３は、それぞれノードＴ２およびＴ３をあるインピーダンスでグラウンドに接続する。ノードＣＴ２およびＣＴ３において受け取られた制御電圧は、それぞれ、抵抗Ｒ２２を介してＦＥＴ　Ｑ２のゲートに、また抵抗Ｒ３２を介してＦＥＴ　Ｑ３のゲートに加えられ、それぞれＦＥＴ　Ｑ２およびＱ３のインピーダンスを変化させる。抵抗Ｒ１２、Ｒ２２およびＲ３２は、ゲートバイアス用の抵抗である。

【００３０】ＦＥＴ　Ｑ１、Ｑ２およびＱ３のソースとグラウンドとの間には、それぞれ抵抗Ｒ１１、Ｒ２１およびＲ３１が設けられている。これらの抵抗Ｒ１１、Ｒ２１およびＲ３１は、それぞれＦＥＴ　Ｑ１、Ｑ２およびＱ３がオン状態のときのノードＴ１、Ｔ２およびＴ３とグラウンドとの間のインピーダンスを調整することによって、インピーダンス整合をとる。

【００３１】ＦＥＴ　Ｑ１と同様に、ＦＥＴ　Ｑ４およびＱ５は、それぞれノードＴ２およびＴ３をあるインピーダンスでノードＴ１に接続する。ノードＣＴ４およびＣＴ５において受け取られた制御電圧は、それぞれ抵抗Ｒ４２を介してＦＥＴ　Ｑ４のゲートに、また抵抗Ｒ５２を介してＦＥＴ　Ｑ５のゲートに加えられ、それぞれＦＥＴＱ４およびＱ５のインピーダンスを変化させる。

【００３２】次にスイッチアッテネータ４０の動作を説明する。スイッチアッテネータ４０は、以下の動作モード１～４を有する。すなわち、

モード１：減衰なしの送信、

11

モード２：減衰ありの送信、
モード３：減衰なしの受信、および
モード４：減衰ありの受信
である。ここで「減衰」とは、ノードＴ１と、ノードＴ２またはノードＴ３との間における減衰をいう。例えばモード１においては、ノードＴ１およびノードＴ２の間の減衰が存在しない。モード１は、ＲＦ部３０を含む移動端末機が基地局から離れている場合、つまり電力増幅器１１６から出力されたＲＦ信号を減衰させることなくアンテナ１３０に供給する場合に用いられる。モード２は、逆にＲＦ部３０を含む移動端末機が基地局に近い場合、つまり電力増幅器１１６から出力されたＲＦ信号を減衰させてからアンテナ１３０に供給する場合に用いられる。送信の場合と同様のことが受信の場合にもあてはまる。モード３は、ＲＦ部３０を含む移動端末機が基地局から離れている場合、つまりアンテナ１３０から入力されたＲＦ信号を減衰させることなく低雑音増幅器１５＊

12

＊２に供給する場合に用いられる。モード４は、逆にＲＦ部３０を含む移動端末機が基地局に近い場合、つまりアンテナ１３０から入力されたＲＦ信号を減衰させてから低雑音増幅器１５２に供給する場合に用いられる。

【００３３】本発明のスイッチアッテネータ４０は、後述するようにモード２およびモード４において、スイッチング素子（ここではＦＥＴ）の制御電圧を変化させることによって、スイッチアッテネータ４０の減衰量を連続的に変化させることができる。その結果、本発明のスイッチアッテネータは、送信時の出力電力、および受信時の入力電力が広いレンジをとりうる移動通信において大きな効果を奏する。

【００３４】（モード１）モード１におけるスイッチアッテネータ４０のＦＥＴ　Ｑ１～Ｑ５の状態を表１に示す。

【００３５】

【表１】

FET	Q1	Q2	Q3	Q4	Q5
状態	オフ	オフ	オン	オン	オフ

【００３６】スイッチアッテネータ４０のモード１を実現するためには、ＦＥＴ　Ｑ１～Ｑ５を表１に示す状態に設定する、それぞれの状態に対応する制御電圧をノードＣＴ１～ＣＴ５に印加すればよい。前述したように、ＦＥＴ　Ｑ１～Ｑ５をオン状態にするためには、例えば０［Ｖ］以上の電圧をそれぞれのゲートに加えればよく、ＦＥＴ　Ｑ１～Ｑ５をオフ状態にするためには、例えばＶＴＨ［Ｖ］以下の電圧をそれぞれのゲートに加えればよい。

【００３７】図５は、モード１におけるスイッチアッテネータ４０の等価回路図である。図５において、閉じたスイッチはオン状態のＦＥＴを表し、開いたスイッチはオフ状態のＦＥＴを表す。モード１においては図５に示すように、ノードＴ１はほぼインピーダンスがゼロでノードＴ２に接続され、ノードＴ３はほぼインピーダンスがゼロでグラウンドに接続され、ノードＴ３は、ノードＴ１およびノードＴ２から遮断されている。したがって※

※モード１においては、電力増幅器１１６から出力されたＲＦ信号は、ノードＴ２において受け取られ、減衰されることなくＦＥＴ　Ｑ４およびノードＴ１を通ってアンテナ１３０に供給される。また低雑音増幅器１５２への入力端子であるノードＴ３は、ＦＥＴ　Ｑ３によってグラウンドに接続され、それにより不要なＲＦ信号が低雑音増幅器１５２へ入力されることを防ぐ。

【００３８】モード１におけるスイッチアッテネータ４０の挿入損失は、ＦＥＴ　Ｑ４のオン状態のインピーダンス（つまりオン抵抗に相当するインピーダンス）に起因する約０．５ｄＢだけである。

【００３９】（モード２）モード２におけるスイッチアッテネータ４０のＦＥＴ　Ｑ１～Ｑ５の状態を表２に示す。

【００４０】

【表２】

FET	Q1	Q2	Q3	Q4	Q5
状態	中間	中間	オン	中間	オフ

【００４１】スイッチアッテネータ４０のモード２を実現するためには、ＦＥＴ　Ｑ１～Ｑ５を表２に示す状態に設定する、それぞれの状態に対応する制御電圧をノードＣＴ１～ＣＴ５に印加すればよい。モード２およびモード４においては、ＦＥＴを中間状態で用いる。ＦＥＴ　Ｑ１～Ｑ５を中間状態にするためには、ゲート・ソース間電圧Ｖｇｓとして、０＜Ｖｇｓ＜ＶＴＨなる電圧をそれぞれのゲートに加えればよい。

【００４２】図６は、モード２におけるスイッチアッテネータ４０の等価回路図である。図６において、閉じたスイッチはオン状態のＦＥＴを表し、開いたスイッチはオフ状態のＦＥＴを表し、抵抗は中間状態のＦＥＴを表す。以下、中間状態のＦＥＴＱ１～Ｑ５のインピーダンスを、それぞれＺＱ１～ＺＱ５のように表すことにする。モード２においては図６に示すように、ノードＴ１はインピーダンスＺＱ４でノードＴ２に接続され、インピーダンスＺＱ１でグラウンドに接続される。ノードＴ２はインピーダンスＺＱ２でグラウンドに接続される。

ノードＴ３はほぼインピーダンスがゼロでグラウンドに接続され、かつノードＴ３は、ノードＴ１およびノードＴ２から遮断されている。したがってモード２においては、電力増幅器１１６から出力されたＲＦ信号は、ノードＴ２において受け取られ、所望の減衰量を伴ってＦＥＴ　Ｑ１、Ｑ２およびＱ４およびノードＴ１を通ってアンテナ１３０に供給される。また低雑音増幅器１５２への入力端子であるノードＴ３は、ＦＥＴ　Ｑ３によってグラウンドに接続され、それにより不要なＲＦ信号が低雑音増幅器１５２へ入力されることを防ぐ。

【００４３】モード２におけるスイッチアッテネータ４０の減衰量は、ＦＥＴ　Ｑ１、Ｑ２およびＱ４のゲートに加えられる制御電圧を変化させること、すなわちインピーダンスＺＱ１、ＺＱ２およびＺＱ４を変化させることによって変わる。ＦＥＴＱ１、Ｑ２およびＱ４のゲートに加えられる制御電圧の値は、例えばあらかじめリードオンリーメモリＲＯＭ１に格納されており、必要な減＊衰量に応じて読み出される。例えばプログラマブルな電圧発生器である制御電圧発生器ＣＶ１がＲＯＭ１から読み出された制御電圧を表すデータに基づいて制御電圧を発生し、それぞれのＦＥＴのゲートに出力すれば、所望の量だけＲＦ信号を減衰させるためのモード２およびモード４を実現できる。またＲＯＭ１は、ＦＥＴ　Ｑ３およびＱ５のゲートに加えられる制御電圧（つまりそれぞれ０［Ｖ］以上の電圧およびＶＴＨ［Ｖ］以下の電圧）を表すデータを併せて格納してもよい。さらにＲＯＭ１は、モード１、３および４においてＦＥＴ　Ｑ１～Ｑ５に加えられる制御電圧を表すデータを併せて格納してもよい。

【００４４】（モード３）モード３におけるスイッチアッテネータ４０のＦＥＴ　Ｑ１～Ｑ５の状態を表３に示す。

【００４５】

【表３】

FET	Q1	Q2	Q3	Q4	Q5
状態	オフ	オン	オフ	オフ	オン

【００４６】スイッチアッテネータ４０のモード３を実現するためには、ＦＥＴ　Ｑ１～Ｑ５を表３に示す状態に設定する、それぞれの状態に対応する制御電圧をノードＣＴ１～ＣＴ５に印加すればよい。

【００４７】図７は、モード３におけるスイッチアッテネータ４０の等価回路図である。モード３においては図７に示すように、ノードＴ１はほぼインピーダンスがゼロでノードＴ３に接続され、ノードＴ２はほぼインピーダンスがゼロでグラウンドに接続され、ノードＴ２は、ノードＴ１およびノードＴ３から遮断されている。したがってモード３においては、アンテナ１３０から入力されたＲＦ信号は、ノードＴ１において受け取られ、減衰されることなくＦＥＴ　Ｑ５およびノードＴ３を通って※低雑音増幅器１５２に供給される。また電力増幅器１１６からの出力端子であるノードＴ２は、ＦＥＴ　Ｑ２によってグラウンドに接続され、それにより不要なＲＦ信号が低雑音増幅器１５２へ出力されることを防ぐ。

【００４８】モード３におけるスイッチアッテネータ４０の挿入損失は、ＦＥＴ　Ｑ５のオン状態のインピーダンスに起因する約０．５ｄＢだけである。

【００４９】（モード４）モード４におけるスイッチアッテネータ４０のＦＥＴ　Ｑ１～Ｑ５の状態を表４に示す。

【００５０】

【表４】

FET	Q1	Q2	Q3	Q4	Q5
状態	中間	オン	中間	オフ	中間

【００５１】スイッチアッテネータ４０のモード４を実現するためには、ＦＥＴ　Ｑ１～Ｑ５を表４に示す状態に設定する、それぞれの状態に対応する制御電圧をノードＣＴ１～ＣＴ５に印加すればよい。

【００５２】図８は、モード４におけるスイッチアッテネータ４０の等価回路図である。モード４においては図８に示すように、ノードＴ１はインピーダンスＺＱ５でノードＴ３に接続され、インピーダンスＺＱ１でグラウンドに接続される。ノードＴ３はインピーダンスＺＱ３でグラウンドに接続される。ノードＴ２はほぼインピーダンスがゼロでグラウンドに接続され、かつノードＴ２は、ノードＴ１およびノードＴ３から遮断されている。したがってモード４においては、アンテナ１３０から入力されたＲＦ信号は、ノードＴ１において受け取られ、所望の減衰量を伴ってＦＥＴ　Ｑ１、Ｑ３およびＱ５およびノードＴ３を通って低雑音増幅器１５２に供給される。また電力増幅器１１６からの出力端子であるノードＴ２は、ＦＥＴ　Ｑ２によってグラウンドに接続され、それにより不要なＲＦ信号が低雑音増幅器１５２へ入力されることを防ぐ。

【００５３】モード４におけるスイッチアッテネータ４０の減衰量は、ＦＥＴ　Ｑ１、Ｑ３およびＱ５のゲートに加えられる制御電圧を変化させること、すなわちインピーダンスＺＱ１、ＺＱ３およびＺＱ５を変化させることによって変わる。ＦＥＴＱ１、Ｑ３およびＱ５のゲートに加えられる制御電圧の値は、モード２で説明したように例えばあらかじめリードオンリーメモリＲＯＭ１に格納されており、必要な減衰量に応じて読み出される。

15

【００５４】第１の実施の形態によればモード２において、実質的にＺＴ１＝ＺＴ２＝Ｚ０なる関係を満たしたままで減衰量を変化させることができる。ここでインピーダンスＺＴ１は、ノードＴ１から見たスイッチアッテネータ４０のインピーダンスを表し、インピーダンスＺＴ２は、ノードＴ２から見たスイッチアッテネータ４０のインピーダンスを表し、インピーダンスＺ０は、外部に接続された回路の特性インピーダンス（例えば５０Ω）を表す。同様に第１の実施の形態によればモード４において、実質的にＺＴ１＝ＺＴ３＝Ｚ０なる関係を満たしたままで減衰量を変化させることができる。ここでインピーダンスＺＴ３は、ノードＴ３から見たスイッチアッテネータ４０のインピーダンスを表す。

【００５５】また上記ＺＴ１＝ＺＴ２＝Ｚ０およびＺＴ１＝ＺＴ３＝Ｚ０なる関係が満たされなくとも、

０．５×ＺＡ≦ＺＴ１≦２．０×ＺＡ、

０．５×ＺＴ≦ＺＴ２≦２．０×ＺＴ、および

０．５×ＺＲ≦ＺＴ３≦２．０×ＺＲ、

という関係が満たされることが好ましい。ここでインピーダンスＺＡは、ノードＴ１に接続される回路（ここではアンテナ１３０）の特性インピーダンスを表し、インピーダンスＺＴは、ノードＴ２に接続される回路（ここでは電力増幅器１１６）の特性インピーダンスを表し、インピーダンスＺＲは、ノードＴ３に接続される回路（ここでは低雑音増幅器１５２）の特性インピーダンスを表す。

【００５６】図９は、半導体基板上に集積化して形成された本発明のスイッチアッテネータ４０の平面図である。図９に示すようにスイッチアッテネータ４０は、ガリウムヒ素（以下「ＧａＡｓ」とする）基板９０１上に集積化されて形成されている。図９の「ＧＮＤ」は、グラウンドを表し、他の参照符号は図４のなかのそれらと対応する。ＦＥＴ　Ｑ１～Ｑ５はＭＥＳＦＥＴであり、ＧａＡｓ基板９０１上にイオン注入法により形成される。ＦＥＴ　Ｑ１～Ｑ５のサイズは、ゲート長が０．５μｍであり、ゲート幅が８００μｍである。図９に示すスイッチアッテネータ４０を実現した半導体チップは、１０ピンの樹脂モールドパッケージに封止されて供用される。

【００５７】（実施の形態２）図１０は、本発明によるスイッチアッテネータの第２の実施形態の回路図である。図１０のＦＥＴ　Ｑ１Ｄ、Ｑ２Ｄ、Ｑ３Ｄ、Ｑ４ＤおよびＱ５Ｄは、デュアルゲートＦＥＴである。ＦＥＴ　Ｑ１Ｄ～Ｑ５Ｄの第１ゲートおよび第２ゲートには、それぞれゲートバイアス抵抗器Ｒ１３およびＲ１４と、Ｒ２３およびＲ２４と、Ｒ３３およびＲ３４と、Ｒ４３およびＲ４４と、Ｒ５３およびＲ５４とが接続されている。またＦＥＴ　Ｑ１Ｄ～Ｑ５Ｄの第２ゲートとドレインとの間には、それぞれコンデンサＣ１３、Ｃ２３、Ｃ３３、Ｃ４３およびＣ５３が接続されており、ＦＥＴ

16

Ｑ１Ｄ～Ｑ５Ｄの第１ゲートとソースとの間には、それぞれコンデンサＣ１４、Ｃ２４、Ｃ３４、Ｃ４４およびＣ５４が接続されている。

【００５８】第２の実施形態は、シングルゲートＦＥＴの代わりにデュアルゲートＦＥＴが用いられていることと、ドレインと第２ゲートとの間、およびソースと第１ゲートとの間にコンデンサが接続されていることとが第１の実施形態と異なる。第２の実施形態の構成によれば、ＦＥＴのもつ非線形性を低減することができ、優れた歪特性を実現できる。

【００５９】（実施の形態３）図１１は、本発明のスイッチアッテネータの第３の実施形態が用いられる携帯電話機のＲＦ部１１００のブロック図である。本発明のスイッチアッテネータ１２００は、送受信の状態に応じて、アンテナ１３０または１３１と、電力増幅器１１６または低雑音増幅器１５２とを電気的に結合する。

【００６０】より具体的には、スイッチアッテネータ１２００は、送信時にはノードＴ１およびＴ４のうちの１つをノードＴ２に電気的に結合し、ノードＴ３をグラウンドに電気的に結合し、ノードＴ１およびＴ４のうちノードＴ２に結合されていないノードを他のノードおよびグラウンドから遮断する。

【００６１】またスイッチアッテネータ１２００は、受信時にはノードＴ１およびＴ４のうちの１つをノードＴ３に電気的に結合し、ノードＴ２をグラウンドに電気的に結合し、ノードＴ１およびＴ４のうちノードＴ３に結合されていないノードを他のノードおよびグラウンドから遮断する。第３の実施形態は、第１の実施形態が単一のアンテナを用いたのと異なり、２つのアンテナ１３０および１３１を利用することができる。したがって第３の実施形態は、第１の実施形態の効果に加えて、２つのアンテナ１３０および１３１を送受信の状況に応じて選択的に利用できるという効果を有する。この第３の実施形態の構成は、例えば空間ダイバーシチ送受信を可能にする。なお図１１のそれぞれのブロックを接続する伝送線路は、すべて５０Ωの特性インピーダンスを有する。

【００６２】図１１および図１２における制御電圧発生器ＣＶ２およびリードオンリーメモリＲＯＭ２は、ＦＥＴを制御する電圧を供給するノードがＣＴ１～ＣＴ８であることを除いて、制御電圧発生器ＣＶ１およびリードオンリーメモリＲＯＭ１と同様に機能する。

【００６３】図１２は、本発明によるスイッチアッテネータの第３の実施形態の回路図である。スイッチアッテネータ１２００は、ノードＴ４を、ノードＴ２およびＴ３のうちの１つに電気的に結合するために、スイッチアッテネータ４０の構成要素に加えて、ＦＥＴ　Ｑ６～Ｑ８と、ゲートバイアス用の抵抗Ｒ６２、Ｒ７２およびＲ８２と、ノードＣＴ６～ＣＴ８と、インピーダンス整合用の抵抗Ｒ６１とをさらに備えている。

【００６４】次にスイッチアッテネータ１２００の動作

17 18

を説明する。スイッチアッテネータ１２００は、以下の動作モード１～８を有する。すなわち、
モード１：アンテナ１３０を用いた減衰なしの送信、
モード２：アンテナ１３０を用いた減衰ありの送信、
モード３：アンテナ１３０を用いた減衰なしの受信、
モード４：アンテナ１３０を用いた減衰ありの受信、
モード５：アンテナ１３１を用いた減衰なしの送信、
モード６：アンテナ１３１を用いた減衰ありの送信、
モード７：アンテナ１３１を用いた減衰なしの受信、および
モード８：アンテナ１３１を用いた減衰ありの受信
である。第３の実施形態のモード１～４は、第１の実施形態のモード１～モード４にそれぞれ対応する。第３の＊実施形態のモード５～８は、ノードＴ１の代わりにノードＴ４がノードＴ２またはＴ３に電気的に結合されることを除き、モード１～４と同じである。

【００６５】スイッチアッテネータ１２００のモード１～８を実現するためには、ＦＥＴＱ１～Ｑ８をそれぞれ以下の表５～表１２に示す状態に設定する、それぞれの状態に対応する制御電圧をノードＣＴ１～ＣＴ８に印加すればよい。スイッチアッテネータ１２００のモード１～モード８の等価回路図をそれぞれ図１３～図２０に示す。

【００６６】
【表５】

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オフ	オン	オン	オフ	オフ	オフ	オフ

【００６７】 ※ ※【表６】

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	中間	中間	オン	中間	オフ	オフ	オフ	オフ

【００６８】 ★ ★【表７】

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オン	オフ	オフ	オン	オフ	オフ	オフ

【００６９】 ☆ ☆【表８】

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	中間	オン	中間	オフ	中間	オフ	オフ	オフ

【００７０】 ◆ ◆【表９】

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オフ	オン	オフ	オフ	オフ	オン	オフ

【００７１】 ＊ ＊【表１０】

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	中間	オン	オフ	オフ	中間	中間	オフ

【００７２】 ※ ※【表１１】

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オン	オフ	オフ	オフ	オフ	オフ	オン

【００７３】 ★ ★【表１２】

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オン	中間	オフ	オフ	中間	オフ	中間

【００７４】第３の実施の形態では、第１の実施の形態と同様に、モード２および４において、それぞれ実質的にＺＴ１＝ＺＴ２＝Ｚ０およびＺＴ１＝ＺＴ３＝Ｚ０なる関係を満たしたままで減衰量を変化させることができる。また第３の実施の形態では、モード６および８において、それぞれ実質的にＺＴ４＝ＺＴ２＝Ｚ０およびＺＴ４＝ＺＴ３＝Ｚ０なる関係を満たしたままで減衰量を変化させることができる。ここでインピーダンスＺＴ４は、ノードＴ４から見たスイッチアッテネータ１２００のインピーダンスを表す。

【００７５】また上記ＺＴ１＝ＺＴ２＝Ｚ０、ＺＴ１＝ＺＴ３＝Ｚ０、ＺＴ４＝ＺＴ２＝Ｚ０およびＺＴ４＝Ｚ

Ｔ３＝Ｚ０なる関係が満たされなくとも、
０．５×ＺＡ≦ＺＴ１≦２．０×ＺＡ、
０．５×ＺＴ≦ＺＴ２≦２．０×ＺＴ、
０．５×ＺＲ≦ＺＴ３≦２．０×ＺＲ、および
０．５×ＺＢ≦ＺＴ４≦２．０×ＺＢ
という関係が満たされることが好ましい。ここでインピーダンスＺＢは、ノードＴ４に接続される回路（ここではアンテナ１３１）の特性インピーダンスを表す。

【００７６】以上説明した第１～第３の実施の形態では、ＦＥＴをオンおよびオフの中間の状態に設定することにより、スイッチアッテネータに接続される回路の特性が変化した場合にも柔軟に対応することができる。このような接続される回路の特性変化は、例えば送信用の電力増幅器から出力される電力を変化させたときなどに起こりうる。

【００７７】上記実施の形態では、例えば携帯電話機と基地局との間の通信で用いられる周波数帯において所望の特性インピーダンスが得られるが、この周波数帯には限定されず、広くＲＦ帯に適用できる。

【００７８】第２の実施の形態の開示に基づいて、第３の実施の形態のＦＥＴをデュアルゲートＦＥＴに置き換えることによって、優れた歪特性が実現できるというさらなる効果を得ることもできる。

【００７９】本発明のスイッチアッテネータに用いられるＦＥＴは、ディプレッション型に限定されず、エンハンスメント型を用いてもよい。またＦＥＴは、上記実施形態ではＭＥＳＦＥＴであるがこれには限定されず、その制御端子によって電気的にインピーダンスを制御できるデバイスであればよい。使用周波数、およびデバイス固有の寄生容量などの条件が許すのであれば、例えばＰＩＮダイオード、ＰＮ接合型ＦＥＴ、ＭＯＳ型ＦＥＴなどを用いてもよい。

【００８０】また本発明によるスイッチアッテネータを電力増幅器または低雑音増幅器とともに半導体基板上に集積化して形成すれば、サイズおよびコストの低減を図ることができ、より好ましい。

【００８１】制御電圧発生器ＣＶ１およびＣＶ２と、リードオンリーメモリＲＯＭ１およびＲＯＭ２とは、本発明によるスイッチアッテネータのＦＥＴの状態をオン状態、中間状態およびオフ状態のいずれかの状態に設定するための制御電圧を発生できるのであれば、上記実施の形態で説明された構成には限られない。例えばデータをディジタル的に格納するメモリをもたない、プログラマブルな電圧発生器を用いてもよい。またリードオンリーメモリＲＯＭ１およびＲＯＭ２の代わりに、ランダムアクセスメモリを用いてもよい。

【００８２】表２、表４、表６、表８、表１０および表１２に示すように、上述の実施の形態では、減衰ありの送信または受信時には、３個のＦＥＴを中間状態に設定している。しかし中間状態のＦＥＴの個数は、３個に限

られず、少なくとも１個のＦＥＴが中間状態であることによって所望の減衰量が得られればよい。

【００８３】

【発明の効果】以上のように本発明によれば、高周波機器において、送信と受信の切り替えや複数のアンテナの切り替えと同時に減衰量を自由に制御することが、一つの半導体素子で実現でき、機器の小型軽量化や低コスト化が図れるという顕著な効果が得られる。

【図面の簡単な説明】

【図１】従来の技術による送受信回路の高周波部１０のブロック図である。

【図２】従来の技術によるスイッチ２０の回路図である。

【図３】本発明のスイッチアッテネータの第１の実施形態が用いられる携帯電話機のＲＦ部３０のブロック図である。

【図４】本発明によるスイッチアッテネータの第１の実施形態の回路図である。

【図５】モード１におけるスイッチアッテネータ４０の等価回路図である。

【図６】モード２におけるスイッチアッテネータ４０の等価回路図である。

【図７】モード３におけるスイッチアッテネータ４０の等価回路図である。

【図８】モード４におけるスイッチアッテネータ４０の等価回路図である。

【図９】半導体基板上に集積化して形成された本発明のスイッチアッテネータ４０の平面図である。

【図１０】本発明によるスイッチアッテネータの第２の実施形態の回路図である。

【図１１】本発明のスイッチアッテネータの第３の実施形態が用いられる携帯電話機のＲＦ部１１００のブロック図である。

【図１２】本発明によるスイッチアッテネータの第３の実施形態の回路図である。

【図１３】モード１におけるスイッチアッテネータ１２００の等価回路図である。

【図１４】モード２におけるスイッチアッテネータ１２００の等価回路図である。

【図１５】モード３におけるスイッチアッテネータ１２００の等価回路図である。

【図１６】モード４におけるスイッチアッテネータ１２００の等価回路図である。

【図１７】モード５におけるスイッチアッテネータ１２００の等価回路図である。

【図１８】モード６におけるスイッチアッテネータ１２００の等価回路図である。

【図１９】モード７におけるスイッチアッテネータ１２００の等価回路図である。

【図２０】モード８におけるスイッチアッテネータ１２

21

００の等価回路図である。

【符号の説明】

４０　スイッチアッテネータ

Ｑ１、Ｑ２、Ｑ３、Ｑ４、Ｑ５　ＦＥＴ

Ｒ１１、Ｒ１２、Ｒ２１、Ｒ２２、Ｒ３１、Ｒ３２、Ｒ＊

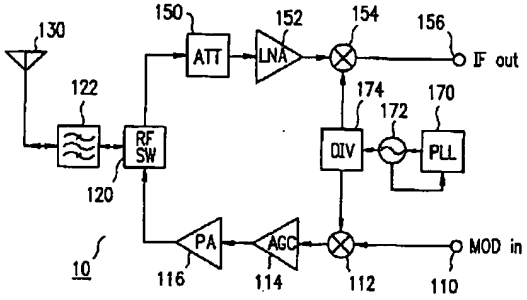
22

＊４２、Ｒ５２　抵抗

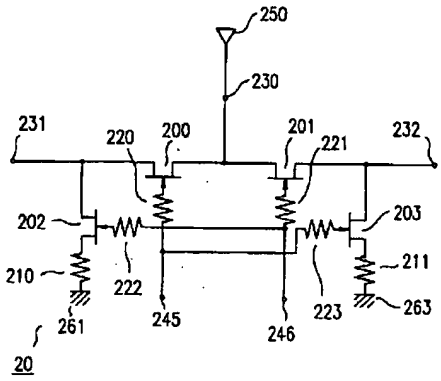
Ｔ１、Ｔ２、Ｔ３、ＣＴ１、ＣＴ２、ＣＴ３、ＣＴ４、ＣＴ５　ノード

１３０　アンテナ

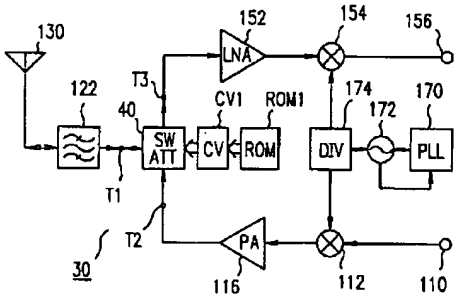
【図１】



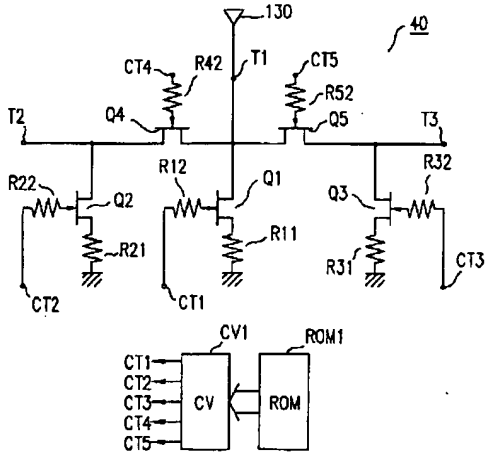
【図２】



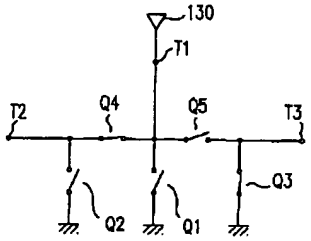
【図３】



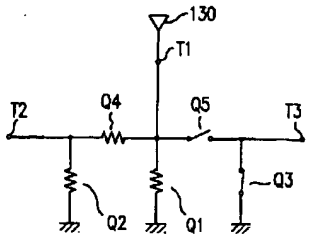
【図４】



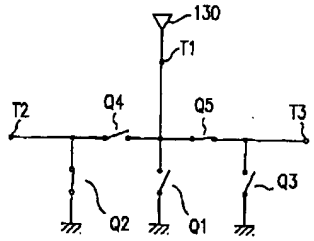
【図５】



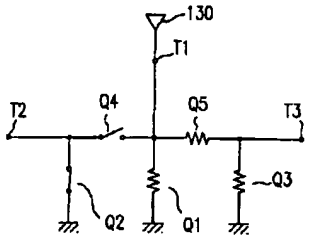
【図６】



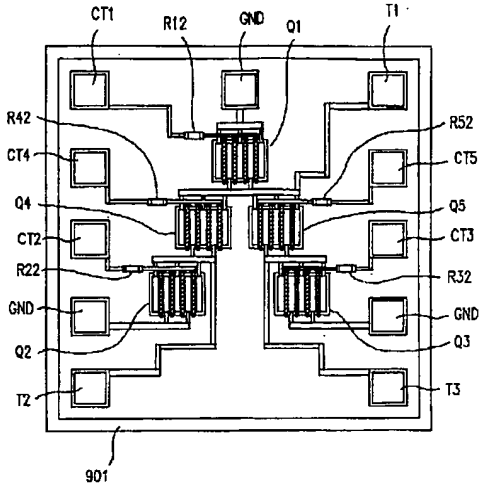
【図７】



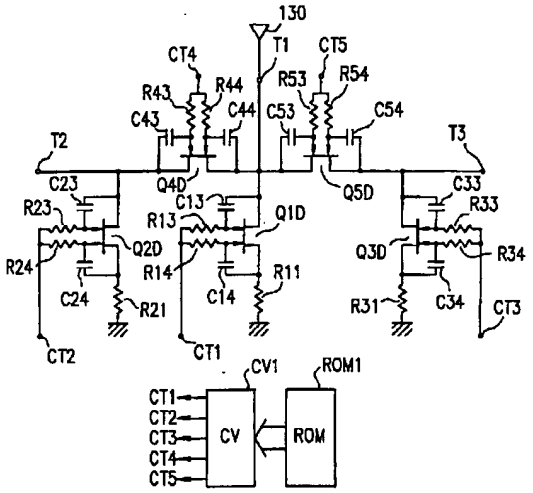
【図８】



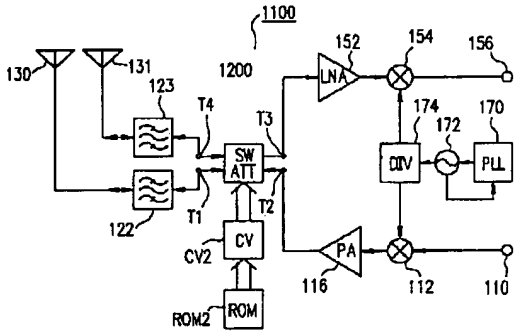
【図９】



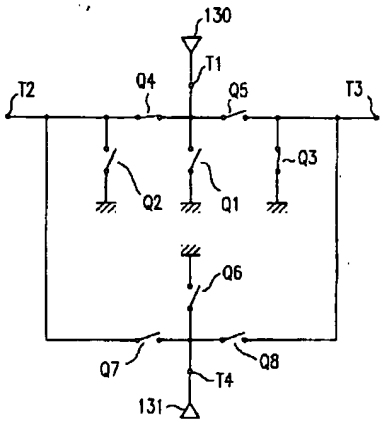
【図１０】



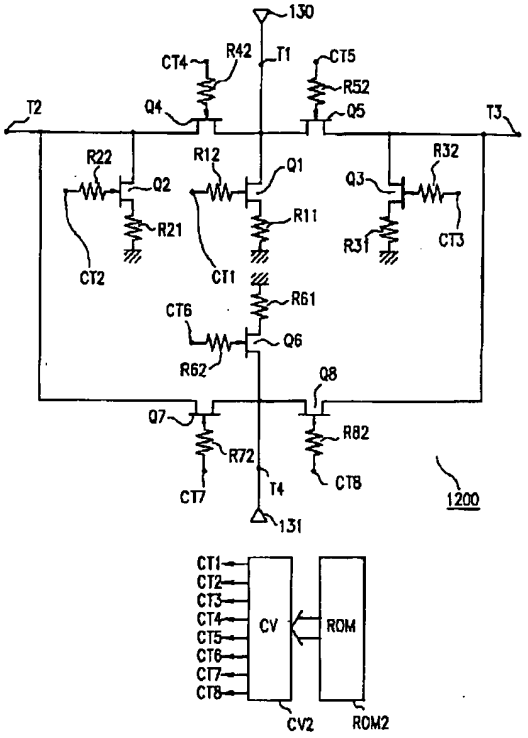
【図１１】



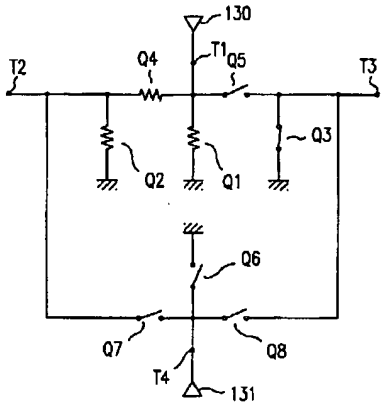
【図１３】



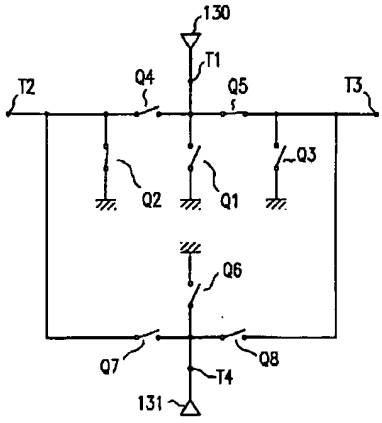
【図１２】



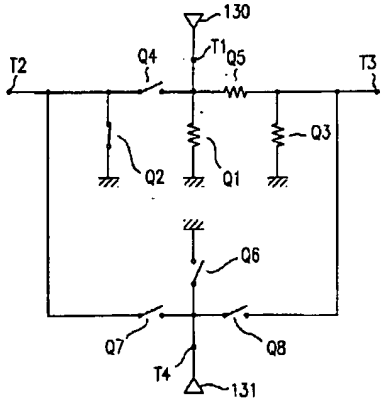
【図１４】



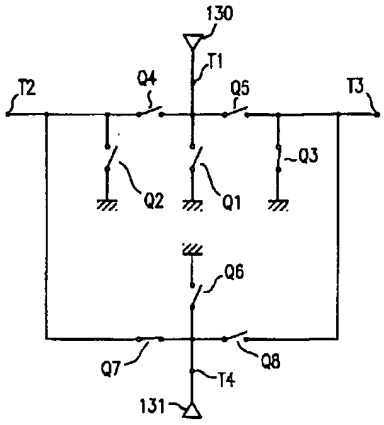
【図１５】



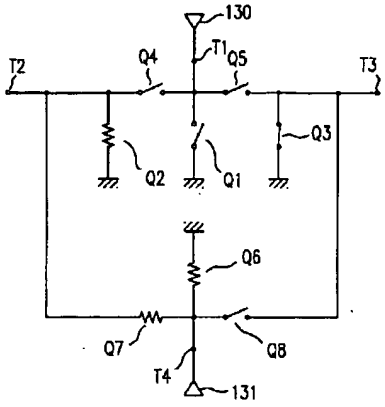
【図１６】



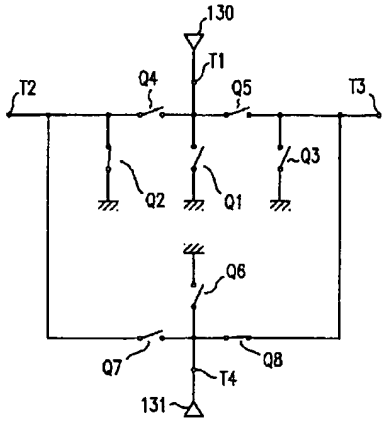
【図１７】



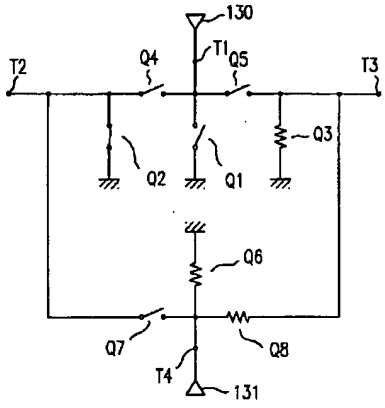
【図１８】



【図１９】



【図２０】



* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] Have the 1st terminal connected to an antenna, the 2nd terminal connected to a transmitter, and the 3rd terminal connected to a receiver, and are the switch attenuator which changes the 1st condition and the 2nd condition, and it sets in this 1st condition. This 1st terminal is connected to this 2nd terminal. This 1st terminal The impedance Z1 which it was intercepted from this 3rd terminal, and this 3rd terminal was connected to the ground, and was seen from this 1st terminal maintaining equal relation substantially to the impedance Z2 seen from this 2nd terminal This switch attenuator is electrically controllable and it sets in this 2nd condition so that the magnitude of attenuation between this 1st terminal and this 2nd terminal may be changed. This 1st terminal It connects with this 3rd terminal and this 1st terminal is intercepted from this 2nd terminal. This 2nd terminal So that it connects with a ground, and the magnitude of attenuation between this 1st terminal and this 3rd terminal may be changed, the impedance Z1 seen from this 1st terminal maintaining equal relation substantially to the impedance Z3 seen from this 3rd terminal This switch attenuator is a controllable switch attenuator electrically.
[Claim 2] The 1st transistor is prepared between said 1st terminal and grounds. The 2nd transistor is prepared between said 2nd terminal and grounds. The 3rd transistor is prepared between said 3rd terminal and grounds. The 4th transistor is prepared between this 1st terminal and this 2nd terminal, the 5th transistor is prepared between this 1st terminal and this 3rd terminal, and it sets in said 1st condition. It is the switch attenuator according to claim 1 this whose 5th transistor this 3rd transistor is an ON state and is an OFF state, this whose 3rd transistor is an ON state in said 2nd condition and this whose 5th transistor is an OFF state.
[Claim 3] Said impedance Z1 is a switch attenuator according to claim 1 to which it is substantially contained in in the range of 0.5xZA-2.0xZA, and said impedance Z2 is substantially contained in in the range of 0.5xZT-2.0xZT, said impedance Z3 is substantially contained in in the range of 0.5xZR-2.0xZR, and ZA, ZT, and ZR express the impedance of said antenna, said transmitter, and said receiver here, respectively.
[Claim 4] Each of said 1st transistor, said 2nd transistor, said 3rd transistor, said 4th transistor, and said 5th transistor the dual gate field-effect transistor which has a drain, the source, and the two gates -- it is -- this -- one gate of the two gates it connects with this drain -- having -- **** -- this -- the gate of another side of the two gates is connected to this source -- having -- **** -- this -- the switch attenuator according to claim 3 from which the two gates receive the electrical potential difference for electric control through resistance, respectively.
[Claim 5] The 1st terminal connected to the 1st antenna, and the 2nd terminal connected to a transmitter, It has the 3rd terminal connected to a receiver, and the 4th terminal connected to the 2nd antenna. Are the switch attenuator which changes the 1st condition, the 2nd condition, the 3rd condition, and the 4th condition, and it sets in this 1st condition. It connects with this 2nd terminal, and this 1st terminal is intercepted from this 3rd terminal. This 3rd terminal Connect with a ground and this 4th terminal is intercepted from this 1st terminal, this 2nd terminal, this 3rd terminal, and this ground. The impedance Z1 seen from this 1st terminal maintaining equal relation substantially to the impedance Z2 seen from this 2nd terminal, so that the magnitude of attenuation between this 1st terminal and this 2nd terminal may be changed This switch attenuator is electrically controllable and it sets in this 2nd condition. It connects with this 3rd terminal, and this 1st terminal is intercepted from this 2nd terminal. This 2nd terminal Connect with a ground and this 4th terminal is intercepted from this 1st terminal, this 2nd terminal, this 3rd terminal, and this ground. The impedance Z1 seen from this 1st terminal maintaining equal relation substantially to the impedance Z3 seen from this 3rd terminal, so that the magnitude of attenuation between this 1st terminal and this 3rd terminal may be changed This switch attenuator is electrically controllable and it sets in this 3rd condition. It connects with this 2nd terminal, and this 4th terminal is intercepted from this 3rd terminal. This 3rd terminal Connect with a ground and this 1st terminal is intercepted from this 2nd terminal, this 3rd terminal, this 4th terminal, and this

ground. The impedance Z4 seen from this 4th terminal maintaining equal relation substantially to the impedance Z2 seen from this 2nd terminal, so that the magnitude of attenuation between this 4th terminal and this 2nd terminal may be changed This switch attenuator is electrically controllable and it sets in this 4th condition. It connects with this 3rd terminal, and this 4th terminal is intercepted from this 2nd terminal. This 2nd terminal Connect with a ground and this 1st terminal is intercepted from this 2nd terminal, this 3rd terminal, this 4th terminal, and this ground. This switch attenuator is a controllable switch attenuator electrically so that the magnitude of attenuation between this 4th terminal and this 3rd terminal may be changed the impedance Z4 seen from this 4th terminal maintaining equal relation substantially to the impedance Z3 seen from this 3rd terminal.

[Claim 6] The 1st transistor is prepared between said 1st terminal and grounds. The 2nd transistor is prepared between said 2nd terminal and grounds. The 3rd transistor is prepared between said 3rd terminal and grounds. The 4th transistor is prepared between this 1st terminal and this 2nd terminal. The 5th transistor It is prepared between this 1st terminal and this 3rd terminal, and the 6th transistor is prepared between said 4th terminal and grounds. The 7th transistor is prepared between this 2nd terminal and this 4th terminal, the 8th transistor is prepared between this 3rd terminal and this 4th terminal, and it sets in said 1st condition. This 3rd transistor is an ON state. This 5th transistor, this 6th transistor, this 7th transistor, and this 8th transistor It is an OFF state and sets in said 2nd condition. This 2nd transistor It is an ON state. This 4th transistor, this 6th transistor, this 7th transistor, and this 8th transistor It is an OFF state and sets in said 3rd condition. This 3rd transistor It is an ON state. This 1st transistor, this 4th transistor, this 5th transistor, and this 8th transistor It is the switch attenuator according to claim 5 this whose 2nd transistor are an OFF state and is an ON state in said 4th condition and this 1st transistor, this 4th transistor, this 5th transistor, and this whose 7th transistor are OFF states.

[Claim 7] Said impedances Z1 and Z4 are substantially contained in the range of 0.5xZA-2.0xZA. Said impedance Z2 It is substantially contained in the range of 0.5xZT-2.0xZT. Said impedance Z3 It is the switch attenuator according to claim 5 to which it is substantially contained in in the range of 0.5xZR-2.0xZR, and ZA, ZT, and ZR express the impedance of said antenna, said transmitter, and said receiver here, respectively.

[Claim 8] A switch attenuator given in either of claim 1 to claims 7 which are integrated and are formed on the semi-conductor substrate.

[Claim 9] It is the switch attenuator according to claim 8 which is further equipped with power amplifier, and this power amplifier is integrated on said semi-conductor substrate, and is formed.

[Claim 10] It is the switch attenuator according to claim 9 which is further equipped with the low noise amplifier, and this low noise amplifier is integrated on said semi-conductor substrate, and is formed.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the switch attenuator containing the high frequency switch and high frequency attenuator which are used for a high frequency transceiver circuit. Moreover, this invention relates to the semiconductor device which realizes this switch attenuator, and the RF device using this semiconductor device.
[0002]
[Description of the Prior Art] Drawing 1 is the block diagram showing the high frequency (referred to as "RF" below) section 10 of the transceiver circuit by the Prior art. The RF section 10 of a transceiver circuit is equipped with the RF switch 120, and, thereby, performs transmission and reception alternatively. At the time of transmission, the signal inputted in the modulating-signal input terminal (MOD in) 110 is radiated from an antenna 130 in space through a frequency converter (it considers as a "mixer" below) 112, a variable gain amplifier (it considers as "AGC amplifier" below) 114, power amplifier (PA) 116, the RF switch (RF SW) 120, and the frequency filter 122.
[0003] Conversely, at the time of reception, the signal received in the antenna 130 is outputted through the frequency filter 122, the RF switch 120, an attenuator 150, a low noise amplifier (LNA) 152, and a mixer 154 from the intermediate frequency (referred to as "IF" below) signal output terminal (IF out) 156.
[0004] transmission and reception -- in any case, a local oscillation signal with a desired frequency is generated, and a phase locked loop (referred to as "PLL" below) 170 and an oscillator 172 output it to a signal distribution box (DIV) 174. By mixing a modulating signal and a local oscillation signal, a mixer 112 generates a RF signal and outputs it to the AGC amplifier 114. By mixing a RF signal and a local oscillation signal, a mixer 154 generates an IF signal and outputs it to the IF signal output terminal 156.
[0005] Actuation of the RF section 10 of drawing 1 is explained below. The RF sections 10 are some mobile transmitters represented by the terminal of a cellular phone. In almost all cases, in a mobile transmitter, the antenna 130 (here, it thinks also including the frequency filter 122) which requires the comparatively big volume for simplification of configuration is used for the both sides of a sending circuit and a receiving circuit. In order to share the antenna section by transmission and reception, at the time of transmission, it is electrically combined with power amplifier 116, and an antenna 130 is electrically separated from a low noise amplifier 152. Conversely, at the time of reception, it dissociates from power amplifier 116 electrically, and an antenna 130 is electrically combined with a low noise amplifier 152. In order to perform the change for such transmission and reception, the semiconductor-device-ized RF switch 120 is usually adopted. The RF switch 120 by the conventional technique uses the transistor as a switching element, and it is controlling it electrically so that a transistor takes the condition of either an ON state and an OFF state.
[0006] Moreover, the terminal (for example, the hand set of a cellular phone itself) in mobile communications transmits a RF signal to a nearby base station, and communicates by receiving a RF signal from a base station. in order to maintain the power received in a base station to about 1 law, according to the distance of a terminal and a base station, it is necessary to control delicately the power transmitted from a terminal In order to maintain almost uniformly the power outputted in the IF signal output terminal 156 of a terminal on the contrary, it is necessary to control RF power inputted into a low noise amplifier 152. In order to fill these demands, generally the RF section 10 of a terminal is equipped with the AGC amplifier 114 for transmission, and the attenuator 150 for reception.
[0007] Drawing 2 is the circuit diagram of the switch 20 by the Prior art. The switch 20 is equipped with field-effect transistors (referred to as "FET" below) 200-203, the resistors 210 and 211 for impedance adjustment, the gate bias resistors 220-223, the antenna terminal 230, the transmitted power-input terminal 231, the received-power output terminal 232, the 1st control terminal 245, and the 2nd control terminal 246 in drawing 2 .

[0008] Actuation of the switch of drawing 2 is explained. At the time of transmission, by impressing a negative larger electrical potential difference than the absolute value of the threshold of FET 201 and 202 to the 2nd control terminal 246, FET 201 and 202 is made into an OFF state, and zero or a forward electrical potential difference is impressed to the 1st control terminal 245, and FET 200 and 203 is made into an ON state. Thereby, transmitted power passes along a terminal 231, FET200, and the antenna terminal 230, and is outputted to an antenna 250.
[0009] Conversely, at the time of reception, by impressing a negative larger electrical potential difference than the absolute value of the threshold of FET 200 and 203 to the 1st control terminal 245, FET 200 and 203 is made into an OFF state, and zero or a forward electrical potential difference is impressed to the 2nd control terminal 246, and FET 201 and 202 is made into an ON state. Thereby, received power passes along an antenna 250, a terminal 230, and FET201, and is outputted to a terminal 232.
[0010]
[Problem(s) to be Solved by the Invention] In the migration terminal equipment of a cellular phone, in order to raise portability, while lightweight[small and]-izing a device, low-cost-izing is important. In order to realize this, the miniaturization and low-cost-izing of a circuit in current and the RF section are called for strongly. However, also in which the above-mentioned conventional technique, the transceiver circuit needed to have a switch, AGC amplifier, and an attenuator separately. Consequently, it had the technical problem that the transceiver circuit by the Prior art had the size of a device, and unescapable increase of cost.
[0011] The place which it is made in order that this invention may solve the above-mentioned technical problem, and is made into the purpose is to offer the equipment which functions as small [which is used for a high frequency transceiver circuit], a light and low cost switch, and an attenuator.
[0012]
[Means for Solving the Problem] The 1st terminal by which the switch attenuator by this invention is connected to an antenna, Have the 2nd terminal connected to a transmitter, and the 3rd terminal connected to a receiver, and are the switch attenuator which changes the 1st condition and the 2nd condition, and it sets in this 1st condition. This 1st terminal is connected to this 2nd terminal. This 1st terminal The impedance Z1 which it was intercepted from this 3rd terminal, and this 3rd terminal was connected to the ground, and was seen from this 1st terminal maintaining equal relation substantially to the impedance Z2 seen from this 2nd terminal This switch attenuator is electrically controllable and it sets in this 2nd condition so that the magnitude of attenuation between this 1st terminal and this 2nd terminal may be changed. This 1st terminal It connects with this 3rd terminal and this 1st terminal is intercepted from this 2nd terminal. This 2nd terminal So that it connects with a ground, and the magnitude of attenuation between this 1st terminal and this 3rd terminal may be changed, the impedance Z1 seen from this 1st terminal maintaining equal relation substantially to the impedance Z3 seen from this 3rd terminal This switch attenuator is electrically controllable and the above-mentioned purpose is attained by that.
[0013] With a certain operation gestalt, the 1st transistor is prepared between said 1st terminal and grounds. The 2nd transistor is prepared between said 2nd terminal and grounds. The 3rd transistor is prepared between said 3rd terminal and grounds. The 4th transistor is prepared between this 1st terminal and this 2nd terminal, the 5th transistor is prepared between this 1st terminal and this 3rd terminal, and it sets in said 1st condition. This 3rd transistor is an ON state, this 5th transistor is an OFF state, in said 2nd condition, this 3rd transistor is an ON state and this 5th transistor is an OFF state.
[0014] With a certain operation gestalt, it is contained substantially [said impedance Z1] in the range of 0.5xZA-2.0xZA, is contained substantially [said impedance Z2] in the range of 0.5xZT-2.0xZT, and is contained substantially [said impedance Z3] in the range of 0.5xZR-2.0xZR, and ZA, ZT, and ZR express the impedance of said antenna, said transmitter, and said receiver here, respectively.
[0015] With a certain operation gestalt, each of said 1st transistor, said 2nd transistor, said 3rd transistor, said 4th transistor, and said 5th transistor the dual gate field-effect transistor which has a drain, the source, and the two gates -- it is -- this -- one gate of the two gates it connects with this drain -- having -- **** -- this -- the gate of another side of the two gates is connected to this source -- having -- **** -- this -- the two gates receive the electrical potential difference for electric control through resistance, respectively.
[0016] The 1st terminal by which the switch attenuator by this invention is connected to the 1st antenna, It has the 2nd terminal connected to a transmitter, the 3rd terminal connected to a receiver, and the 4th terminal connected to the 2nd antenna. Are the switch attenuator which changes the 1st condition, the 2nd condition, the 3rd condition, and the 4th condition, and it sets in this 1st condition. It connects with this 2nd terminal, and this 1st terminal is intercepted from this 3rd terminal. This 3rd terminal Connect with a ground and this 4th terminal is intercepted from

this 1st terminal, this 2nd terminal, this 3rd terminal, and this ground. The impedance Z1 seen from this 1st terminal maintaining equal relation substantially to the impedance Z2 seen from this 2nd terminal, so that the magnitude of attenuation between this 1st terminal and this 2nd terminal may be changed This switch attenuator is electrically controllable and it sets in this 2nd condition. It connects with this 3rd terminal, and this 1st terminal is intercepted from this 2nd terminal. This 2nd terminal Connect with a ground and this 4th terminal is intercepted from this 1st terminal, this 2nd terminal, this 3rd terminal, and this ground. The impedance Z1 seen from this 1st terminal maintaining equal relation substantially to the impedance Z3 seen from this 3rd terminal, so that the magnitude of attenuation between this 1st terminal and this 3rd terminal may be changed This switch attenuator is electrically controllable and it sets in this 3rd condition. It connects with this 2nd terminal, and this 4th terminal is intercepted from this 3rd terminal. This 3rd terminal Connect with a ground and this 1st terminal is intercepted from this 2nd terminal, this 3rd terminal, this 4th terminal, and this ground. The impedance Z4 seen from this 4th terminal maintaining equal relation substantially to the impedance Z2 seen from this 2nd terminal, so that the magnitude of attenuation between this 4th terminal and this 2nd terminal may be changed This switch attenuator is electrically controllable and it sets in this 4th condition. It connects with this 3rd terminal, and this 4th terminal is intercepted from this 2nd terminal. This 2nd terminal Connect with a ground and this 1st terminal is intercepted from this 2nd terminal, this 3rd terminal, this 4th terminal, and this ground. The impedance Z4 seen from this 4th terminal maintaining equal relation substantially to the impedance Z3 seen from this 3rd terminal, so that the magnitude of attenuation between this 4th terminal and this 3rd terminal may be changed This switch attenuator is electrically controllable and the above-mentioned purpose is attained by that.

[0017] With a certain operation gestalt, the 1st transistor is prepared between said 1st terminal and grounds. The 2nd transistor is prepared between said 2nd terminal and grounds. The 3rd transistor is prepared between said 3rd terminal and grounds. The 4th transistor is prepared between this 1st terminal and this 2nd terminal. The 5th transistor It is prepared between this 1st terminal and this 3rd terminal, and the 6th transistor is prepared between said 4th terminal and grounds. The 7th transistor is prepared between this 2nd terminal and this 4th terminal, the 8th transistor is prepared between this 3rd terminal and this 4th terminal, and it sets in said 1st condition. This 3rd transistor is an ON state. This 5th transistor, this 6th transistor, this 7th transistor, and this 8th transistor It is an OFF state and sets in said 2nd condition. This 2nd transistor It is an ON state. This 4th transistor, this 6th transistor, this 7th transistor, and this 8th transistor It is an OFF state and sets in said 3rd condition. This 3rd transistor It is an ON state. This 1st transistor, this 4th transistor, this 5th transistor, and this 8th transistor It is an OFF state, and in said 4th condition, this 2nd transistor is an ON state and this 1st transistor, this 4th transistor, this 5th transistor, and this 7th transistor are OFF states.

[0018] With a certain operation gestalt, it is contained substantially [said impedances Z1 and Z4] in the range of 0.5xZA-2.0xZA, is contained substantially [said impedance Z2] in the range of 0.5xZT-2.0xZT, and is contained substantially [said impedance Z3] in the range of 0.5xZR-2.0xZR, and ZA, ZT, and ZR express the impedance of said antenna, said transmitter, and said receiver here, respectively.

[0019] With a certain operation gestalt, on the semi-conductor substrate, it integrates and is formed.

[0020] With a certain operation gestalt, it has power amplifier further, and this power amplifier is integrated and formed on said semi-conductor substrate.

[0021] With a certain operation gestalt, it has the low noise amplifier further, and this low noise amplifier is integrated and formed on said semi-conductor substrate.

[0022]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained, referring to a drawing. The same reference mark expresses the same component.

[0023] The "switch attenuator" in this specification says the equipment it has equipment and the function of RF switch for antennas, and RF attenuator so that it may mention later. Moreover, a "node" does not necessarily need the terminal for connection with the equipment exterior.

[0024] (Gestalt 1 of operation) Drawing 3 is the block diagram of the RF section 30 of the portable telephone with which the 1st operation gestalt of the switch attenuator of this invention is used. The switch attenuator 40 of this invention combines electrically an antenna 130, and power amplifier 116 or a low noise amplifier 152 according to the condition of transmission and reception. The switch attenuator 40 combines a node T1 with a node T2 electrically at the time of transmission, and, more specifically, combines node T3 with a ground electrically. Moreover, the switch attenuator 40 combines a node T1 with node T3 electrically at the time of reception, and combines a node T2 with a ground electrically. The ground in this specification is connected to the case shielded in RF while the negative

electrode of a power source is connected and it offers common potential about the both sides of a direct-current (referred to as "DC" below) signal, and a RF signal. The flow of the signal at the time of the transmission and reception in the RF section 30 is the same as drawing 1 explained.

[0025] Since the switch attenuator 40 by this invention has a switch and the function of an attenuator so that it may mention later, it has the big effectiveness that the AGC amplifier 114 and attenuator 150 of drawing 1 can be lost. Moreover, if it manufactures as a semiconductor device which had the switch attenuator 40 unified, drastic reduction of size and cost is more desirable than a possible next door. In addition, all the transmission lines that connect each block of drawing 3 have the characteristic impedance of 50 ohms. Moreover, although the RF section 30 is used as some portable telephones, it is not limited to this here. The RF section 30 can be widely used for the equipment which transmits and receives a RF signal, and it can use the switch attenuator 40 widely as equipment to attenuate while changing a RF signal.

[0026] In drawing 3 , the control voltage generator valve flow coefficient 1 is generated based on the data in which the control voltage for setting up the condition of FET contained in the switch attenuator 40 as shown in Table 1 - 4 explained later was stored by the read only memory ROM 1, and is supplied to each FET. A read only memory ROM 1 stores the data for generating the control voltage of FET corresponding to the condition of Table 1 - 4.

[0027] Drawing 4 is the circuit diagram of the 1st operation gestalt of the switch attenuator by this invention. The switch attenuator 40 is equipped with nodes T1 and T2 and T3, and is connected to an antenna 130, power amplifier 116, and a low noise amplifier 152, respectively. The control voltage generator valve flow coefficient 1 generates the electrical potential difference which controls FET based on the data stored in the read only memory ROM 1, and outputs it to nodes CT1-CT5.

[0028] FET Q1 connects a node T1 to a ground with a certain impedance. The control voltage received in the node CT 1 minds resistance R12, and is FET. It is added to the gate of Q1 and is FET. This predetermined impedance of Q1 is changed. It responds to the control voltage of a node CT 1, and, specifically, is FET. Q1 can take the impedance of the large range from an ON state to an OFF state. FET In an ON state, the impedance of Q1 is low to extent it can consider that is zero, and high to extent it can consider that is infinite in an OFF state. FET Since it is the depletion type of N type, Q1 is FET. It is FET conversely that what is necessary is just to give the electrical potential difference Vgs between the gate sources more than 0 [V] in order to make Q1 into an ON state. What is necessary is just to give the electrical potential difference Vgs between the gate sources below a threshold VTH [V] (VTH<0), in order to make Q1 into an OFF state. FET When filling the relation which the electrical potential difference Vgs between the gate sources of Q1 becomes VTH<Vgs<0, it sets on these specifications, and it is FET. Q1 is made to call that it is the "intermediate state" of an ON state and an OFF state. FET Q1 is the Schottky barrier gate mold FET (referred to as "MESFET" below) with the gestalt of this operation. As mentioned above, FET It sets on these specifications and the explanation about Q1 is FET. It is applied also about Q2-Q4.

[0029] FET It is FET like Q1. Q2 and Q3 connect a node T2 and T3 to a ground with a certain impedance, respectively. The control voltage received in nodes CT2 and CT3 minds resistance R22, and is FET, respectively. Resistance R32 is minded [of Q2] again, and it is FET. It is added to the gate of Q3 and is FET, respectively. The impedance of Q2 and Q3 is changed. Resistance R12, R22, and R32 is resistance for gate bias.

[0030] FET Between the source of Q1, Q2, and Q3, and a ground, resistance R11, R21, and R31 is formed, respectively. These resistance R11, R21, and R31 is FET, respectively. Impedance matching is taken by adjusting the nodes T1 and T2 in case Q1, Q2, and Q3 are ON states, and the impedance between T3 and a ground.

[0031] FET It is FET like Q1. Q4 and Q5 connect a node T2 and T3 to a node T1 with a certain impedance, respectively. The control voltage received in nodes CT4 and CT5 minds resistance R42, respectively, and is FET. Resistance R52 is minded [of Q4] again, and it is FET. It is added to the gate of Q5 and the impedance of FETQ4 and Q5 is changed, respectively.

[0032] Next, actuation of the switch attenuator 40 is explained. The switch attenuator 40 has the following modes of operation 1-4. Namely, transmission without mode 1:attenuation, transmission with mode 2:attenuation, the reception without mode 3:attenuation, and the mode 4: It is reception with attenuation. Attenuation between a node T1, and a node T2 or node T3 of "attenuation" is said here. For example, in the mode 1, attenuation between a node T1 and a node T2 does not exist. The mode 1 is used when the migration terminal containing the RF section 30 is distant from the base station (i.e., when supplying an antenna 130, without attenuating the RF signal outputted from power amplifier 116). The mode 2 is used when the migration terminal which contains the RF section 30 conversely is close to a base station (i.e., since the RF signal outputted from power amplifier 116 is attenuated when supplying an antenna 130). It is applied also when it is reception that it is the same as that of the case of transmission. The mode

3 is used when the migration terminal containing the RF section 30 is distant from the base station (i.e., when supplying a low noise amplifier 152, without attenuating the RF signal inputted from the antenna 130). The mode 4 is used when the migration terminal which contains the RF section 30 conversely is close to a base station (i.e., since the RF signal inputted from the antenna 130 is attenuated when supplying a low noise amplifier 152).
[0033] The switch attenuator 40 of this invention can change the magnitude of attenuation of the switch attenuator 40 continuously by changing the control voltage of a switching element (here FET) in the mode 2 and the mode 4 so that it may mention later. Consequently, the switch attenuator of this invention does big effectiveness so in the mobile communication which can take a range with large output power at the time of transmission and input power at the time of reception.
[0034] (Mode 1) FET of the switch attenuator 40 in the mode 1 The condition of Q1-Q5 is shown in Table 1.
[0035]
[Table 1]

FET	Q1	Q2	Q3	Q4	Q5
状態	オフ	オフ	オン	オン	オフ

[0036] It is FET in order to realize the mode 1 of the switch attenuator 40. What is necessary is just to impress the control voltage corresponding to each condition of setting Q1-Q5 as the condition which shows in Table 1 to nodes CT1-CT5. It is FET as mentioned above. It is FET that what is necessary is just to apply the electrical potential difference for example, more than 0 [V] to each gate in order to make Q1-Q5 into an ON state. What is necessary is just to apply the electrical potential difference for example, below VTH [V] to each gate, in order to make Q1-Q5 into an OFF state.
[0037] Drawing 5 is the representative circuit schematic of the switch attenuator 40 in the mode 1. In drawing 5 , the closed switch expresses FET of an ON state and the open switch expresses FET of an OFF state. As the mode 1 is shown in drawing 5 , an impedance is mostly connected to a node T2 by zero, as for node T3, an impedance is mostly connected to a ground by zero, and node T3 is intercepted for the node T1 from the node T1 and the node T2. Therefore, the RF signal outputted from power amplifier 116 in the mode 1 is FET, without receiving and decreasing in a node T2. An antenna 130 is supplied through Q4 and a node T1. Moreover, node T3 which is an input terminal to a low noise amplifier 152 is FET. It prevents Q's3 connecting with a ground and an unnecessary RF signal being inputted by that cause into a low noise amplifier 152.
[0038] The insertion loss of the switch attenuator 40 in the mode 1 is FET. It is only about 0.5dB resulting from the impedance (that is, impedance equivalent to on resistance) of the ON state of Q4.
[0039] (Mode 2) FET of the switch attenuator 40 in the mode 2 The condition of Q1-Q5 is shown in Table 2.
[0040]
[Table 2]

FET	Q1	Q2	Q3	Q4	Q5
状態	中間	中間	オン	中間	オフ

[0041] It is FET in order to realize the mode 2 of the switch attenuator 40. What is necessary is just to impress the control voltage corresponding to each condition of setting Q1-Q5 as the condition which shows in Table 2 to nodes CT1-CT5. In the mode 2 and the mode 4, FET is used by the intermediate state. FET What is necessary is just to apply to each gate the electrical potential difference which becomes 0<Vgs<VTH as an electrical potential difference Vgs between the gate sources, in order to make Q1-Q5 into an intermediate state.
[0042] Drawing 6 is the representative circuit schematic of the switch attenuator 40 in the mode 2. In drawing 6 , the closed switch expresses FET of an ON state, the open switch expresses FET of an OFF state, and resistance expresses FET of an intermediate state. Hereafter, the impedance of FETQ1-Q5 of an intermediate state is made to express like ZQ1-ZQ5, respectively. As the mode 2 is shown in drawing 6 , it connects with a node T2 with an impedance ZQ4, and a node T1 is connected to a ground with an impedance ZQ1. A node T2 is connected to a ground with an impedance ZQ2. As for node T3, an impedance is mostly connected to a ground by zero, and node T3 is intercepted from the node T1 and the node T2. Therefore, it is received in a node T2, it is accompanied by the desired magnitude of attenuation, and the RF signal outputted from power amplifier 116 in the mode 2 is FET. An antenna 130 is supplied through Q1, Q2, Q4, and a node T1. Moreover, node T3 which is an input terminal to a low noise amplifier 152 is FET. It prevents Q's3 connecting with a ground and an unnecessary RF signal being inputted by

that cause into a low noise amplifier 152.
[0043] The magnitude of attenuation of the switch attenuator 40 in the mode 2 is FET. It changes changing the control voltage applied to the gate of Q1, Q2, and Q4, i.e., by changing impedances ZQ1, ZQ2, and ZQ4. The value of the control voltage applied to the gate of FETQ1, Q2, and Q4 is beforehand stored in the read only memory ROM 1, for example, and is read according to the required magnitude of attenuation. For example, if the control voltage generator valve flow coefficient 1 which is a programmable voltage generator generates control voltage based on the data showing the control voltage read from ROM1 and outputs to the gate of each FET, the mode 2 and the mode 4 only for a desired amount to attenuate a RF signal are realizable. Moreover, ROM1 is FET. The data showing the control voltage (that is, the electrical potential difference more than each 0 [V] and the electrical potential difference below VTH [V]) applied to the gate of Q3 and Q5 may be stored collectively. Furthermore, it sets in the modes 1, 3, and 4, and ROM1 is FET. The data showing the control voltage applied to Q1-Q5 may be stored collectively.
[0044] (Mode 3) FET of the switch attenuator 40 in the mode 3 The condition of Q1-Q5 is shown in Table 3.
[0045]
[Table 3]

FET	Q1	Q2	Q3	Q4	Q5
状態	オフ	オン	オフ	オフ	オン

[0046] It is FET in order to realize the mode 3 of the switch attenuator 40. What is necessary is just to impress the control voltage corresponding to each condition of setting Q1-Q5 as the condition which shows in Table 3 to nodes CT1-CT5.
[0047] Drawing 7 is the representative circuit schematic of the switch attenuator 40 in the mode 3. As the mode 3 is shown in drawing 7 R> 7, an impedance is mostly connected to node T3 by zero, mostly, an impedance is connected to a ground by zero and the node T2 is intercepted [the node T2] for the node T1 from a node T1 and node T3. Therefore, the RF signal inputted from the antenna 130 in the mode 3 is FET, without receiving and decreasing in a node T1. A low noise amplifier 152 is supplied through Q5 and node T3. Moreover, the node T2 which is an output terminal from power amplifier 116 is FET. It prevents Q's2 connecting with a ground and an unnecessary RF signal being outputted by that cause to a low noise amplifier 152.
[0048] The insertion loss of the switch attenuator 40 in the mode 3 is FET. It is only about 0.5dB resulting from the impedance of the ON state of Q5.
[0049] (Mode 4) FET of the switch attenuator 40 in the mode 4 The condition of Q1-Q5 is shown in Table 4.
[0050]
[Table 4]

FET	Q1	Q2	Q3	Q4	Q5
状態	中間	オン	中間	オフ	中間

[0051] It is FET in order to realize the mode 4 of the switch attenuator 40. What is necessary is just to impress the control voltage corresponding to each condition of setting Q1-Q5 as the condition which shows in Table 4 to nodes CT1-CT5.
[0052] Drawing 8 is the representative circuit schematic of the switch attenuator 40 in the mode 4. As the mode 4 is shown in drawing 8 R> 8, it connects with node T3 with an impedance ZQ5, and a node T1 is connected to a ground with an impedance ZQ1. Node T3 is connected to a ground with an impedance ZQ3. Mostly, an impedance is connected to a ground by zero, and the node T2 is intercepted for the node T2 from a node T1 and node T3. Therefore, it is received in a node T1, it is accompanied by the desired magnitude of attenuation, and the RF signal inputted from the antenna 130 in the mode 4 is FET. A low noise amplifier 152 is supplied through Q1, Q3, Q5, and node T3. Moreover, the node T2 which is an output terminal from power amplifier 116 is FET. It prevents Q's2 connecting with a ground and an unnecessary RF signal being inputted by that cause into a low noise amplifier 152.
[0053] The magnitude of attenuation of the switch attenuator 40 in the mode 4 is FET. It changes changing the control voltage applied to the gate of Q1, Q3, and Q5, i.e., by changing impedances ZQ1, ZQ3, and ZQ5. The value of the control voltage applied to the gate of FETQ1, Q3, and Q5 is beforehand stored in the read only memory ROM 1, as explained in the mode 2, and it is read according to the required magnitude of attenuation.
[0054] The magnitude of attenuation can be changed filling the relation it is substantially unrelated ZT1=ZT2=Z0 in the mode 2 according to the gestalt of the 1st operation. An impedance ZT1 expresses the impedance of the switch

attenuator 40 seen from the node T1, an impedance ZT2 expresses the impedance of the switch attenuator 40 seen from the node T2, and an impedance Z0 expresses the characteristic impedance (for example, 50ohms) of the circuit connected outside here. The magnitude of attenuation can be changed filling similarly the relation it is substantially unrelated ZT1=ZT3=Z0 in the mode 4 according to the gestalt of the 1st operation. An impedance ZT3 expresses the impedance of the switch attenuator 40 seen from node T3 here.

[0055] Moreover, even if above-mentioned ZT1=ZT2=Z0 and the relation it is unrelated ZT1=ZT3=Z0 are not filled, it is desirable that relation called 0.5xZA<=ZT1 <=2.0xZA, 0.5xZT<=ZT2 <=2.0xZT, and 0.5xZR<=ZT3 <=2.0xZR is filled. An impedance ZA expresses the characteristic impedance of the circuit (here antenna 130) connected to a node T1, an impedance ZT expresses the characteristic impedance of the circuit (here power amplifier 116) connected to a node T2, and an impedance ZR expresses the characteristic impedance of the circuit (here low noise amplifier 152) connected to node T3 here.

[0056] Drawing 9 is the top view of the switch attenuator 40 of this invention integrated and formed on the semi-conductor substrate. As shown in drawing 9 , the switch attenuator 40 is integrated and formed on the gallium-arsenide (referred to as "GaAs" below) substrate 901. "GND" of drawing 9 expresses a ground and other reference marks correspond with them in drawing 4 . FET Q1-Q5 are MESFET(s), and they are formed by ion-implantation on the GaAs substrate 901. FET Gate length is 0.5 micrometers and the gate width of the size of Q1-Q5 is 800 micrometers. The closure of the semiconductor chip which realized the switch attenuator 40 shown in drawing 9 is carried out to the resin mold package of ten pins, and it is made available.

[0057] (Gestalt 2 of operation) Drawing 10 is the circuit diagram of the 2nd operation gestalt of the switch attenuator by this invention. FET of drawing 10 Q1D, Q2D, Q3D, Q4D, and Q5D are dual gate FET. FET The gate bias resistors R13 and R14, R23 and R24, R33 and R34, R43 and R44, and R53 and R54 are connected to the 1st gate and the 2nd gate of Q1 D-Q5D, respectively. Moreover, FET Between the 2nd gate of Q1D - Q5D, and a drain, capacitors C13, C23, C33, C43, and C53 are connected, respectively, and it is FET. Between the 1st gate of Q1 D-Q5D, and the source, capacitors C14, C24, C34, C44, and C54 are connected, respectively.

[0058] As for the 2nd operation gestalt, it differs from the 1st operation gestalt that the capacitor is connected between that dual gate FET is used instead of, and a drain and the 2nd gate and between the source and the 1st gate. [a single gate FET] According to the configuration of the 2nd operation gestalt, the nonlinearity which FET has can be reduced and the outstanding distorted property can be realized.

[0059] (Gestalt 3 of operation) Drawing 11 is the block diagram of the RF section 1100 of the portable telephone with which the 3rd operation gestalt of the switch attenuator of this invention is used. The switch attenuator 1200 of this invention combines electrically antennas 130 or 131, and power amplifier 116 or a low noise amplifier 152 according to the condition of transmission and reception.

[0060] More specifically, the switch attenuator 1200 intercepts the node which one is electrically combined with a node T2 of a node T1 and the T four at the time of transmission, combines node T3 with a ground electrically, and is not combined with a node T2 among a node T1 and T four from other nodes and grounds.

[0061] Moreover, the switch attenuator 1200 intercepts the node which one is electrically combined with node T3 of a node T1 and the T four at the time of reception, combines a node T2 with a ground electrically, and is not combined with node T3 among a node T1 and T four from other nodes and grounds. Unlike having used the antenna with the 1st single operation gestalt, the 3rd operation gestalt can use two antennas 130 and 131. Therefore, in addition to the effectiveness of the 1st operation gestalt, the 3rd operation gestalt has the effectiveness that two antennas 130 and 131 can be alternatively used according to the situation of transmission and reception. The configuration of this 3rd operation gestalt enables for example, space diversity transmission and reception. In addition, all the transmission lines that connect each block of drawing 11 have the characteristic impedance of 50 ohms.

[0062] The control voltage generator valve flow coefficient 2 in drawing 11 and drawing 12 and a read only memory ROM 2 function as the control voltage generator valve flow coefficient 1 and a read only memory ROM 1 similarly except for the nodes which supply the electrical potential difference which controls FET being CT1-CT8.

[0063] Drawing 12 is the circuit diagram of the 3rd operation gestalt of the switch attenuator by this invention. In order to join together electrically of a node T2 and T3 to one, the switch attenuator 1200 adds node T four to the component of the switch attenuator 40, and is FET. It has further Q6-Q8, the resistance R62, R72, and R82 for gate bias, nodes CT6-CT8, and the resistance R61 for impedance matching.

[0064] Next, actuation of the switch attenuator 1200 is explained. The switch attenuator 1200 has the following modes of operation 1-8. Namely, the transmission without attenuation using the mode 1:antenna 130, the mode 2 :

The transmission with attenuation using an antenna 130, Mode 3 : The reception without attenuation using an antenna 130, the reception with attenuation using the mode 4:antenna 130, mode 5: -- they are the transmission without attenuation using an antenna 131, the transmission with attenuation using the mode 6:antenna 131, the reception without attenuation using the mode 7:antenna 131, and reception with attenuation using the mode 8:antenna 131. The modes 1-4 of the 3rd operation gestalt are equivalent to the mode 1 of the 1st operation gestalt - the mode 4, respectively. Node T four of the modes 5-8 of the 3rd operation gestalt is the same as that of the modes 1-4 except for being electrically combined with a node T2 or T3 instead of a node T1.

[0065] What is necessary is just to impress the control voltage corresponding to each condition of setting FETQ1-Q8 as the condition which shows in following Table 5 - 12, respectively to nodes CT1-CT8, in order to realize the modes 1-8 of the switch attenuator 1200. The representative circuit schematic in the mode 1 of the switch attenuator 1200 - the mode 8 is shown in drawing 13 - drawing 20 , respectively.

[0066]

[Table 5]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オフ	オン	オン	オフ	オフ	オフ	オフ

[0067]

[Table 6]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	中間	中間	オン	中間	オフ	オフ	オフ	オフ

[0068]

[Table 7]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オン	オフ	オフ	オン	オフ	オフ	オフ

[0069]

[Table 8]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	中間	オン	中間	オフ	中間	オフ	オフ	オフ

[0070]

[Table 9]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オフ	オン	オフ	オフ	オフ	オン	オフ

[0071]

[Table 10]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	中間	オン	オフ	オフ	中間	中間	オフ

[0072]

[Table 11]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オン	オフ	オフ	オフ	オフ	オフ	オン

[0073]

[Table 12]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オン	中間	オフ	オフ	中間	オフ	中間

[0074] With the gestalt of the 3rd operation, the magnitude of attenuation can be changed like the gestalt of the 1st operation, filling substantially ZT1=ZT2=Z0 and the relation it is unrelated ZT1=ZT3=Z0 in the modes 2 and 4, respectively. Moreover, with the gestalt of the 3rd operation, the magnitude of attenuation can be changed in the modes 6 and 8, filling substantially ZT4=ZT2=Z0 and the relation it is unrelated ZT4=ZT3=Z0, respectively. An impedance ZT4 expresses the impedance of the switch attenuator 1200 seen from node T four here.
[0075] Moreover, even if the above-mentioned ZT1=ZT2=Z0, ZT1=ZT3=Z0, ZT4=ZT2=Z0, and the relation it is unrelated ZT4=ZT3=Z0 are not filled, it is desirable that relation called 0.5xZA<=ZT1 <=2.0xZA, 0.5xZT<=ZT2 <=2.0xZT, 0.5xZR<=ZT3 <=2.0xZR, and 0.5xZB<=ZT4 <=2.0xZB is filled. An impedance ZB expresses the characteristic impedance of the circuit (here antenna 131) connected to node T four here.
[0076] With the gestalt of the 1st explained above - the 3rd operation, by setting FET as the middle condition of ON and OFF, also when the property of the circuit connected to a switch attenuator changes, it can respond flexibly. Such property change of the circuit connected may take place, when changing the power outputted from the power amplifier for transmission.
[0077] Although a desired characteristic impedance is obtained with the gestalt of the above-mentioned implementation in the frequency band used, for example by the communication link between a portable telephone and a base station, it is not limited to this frequency band, but can apply to RF band widely.
[0078] Based on the indication of the gestalt of the 2nd operation, the further effectiveness that the outstanding distorted property is realizable can also be acquired by transposing FET of the gestalt of the 3rd operation to dual gate FET.
[0079] FET used for the switch attenuator of this invention is not limited to a depletion type, but an enhancement type may be used for it. Moreover, FET should just be the device which is not limited to this although it is MESFET, but can control an impedance by the above-mentioned operation gestalt electrically with the control terminal. As long as conditions, such as an operating frequency and parasitic capacitance of a device proper, allow, a PIN diode, the PN-junction mold FET, a MOSFET, etc. may be used, for example.
[0080] Moreover, if the switch attenuator by this invention is integrated and formed on a semi-conductor substrate with power amplifier or a low noise amplifier, reduction of size and cost can be aimed at and it is more desirable.
[0081] The control voltage generators valve flow coefficient1 and valve flow coefficient2 and read only memories ROM1 and ROM2 will not be restricted to the configuration explained with the gestalt of the above-mentioned implementation, if the control voltage for setting the condition of FET of the switch attenuator by this invention as the condition of either an ON state, an intermediate state and an OFF state can be generated. For example, a programmable voltage generator without the memory which stores data in digital one may be used. Moreover, random access memory may be used instead of read only memories ROM1 and ROM2.
[0082] As shown in Table 2, Table 4, Table 6, and Table 8, 10, and 12, with the gestalt of above-mentioned operation, three FET is set as an intermediate state at the time of the transmission with attenuation, or reception. However, the number of FET of an intermediate state is not restricted to three pieces, but when at least one FET is an intermediate state, the desired magnitude of attenuation should just be obtained.
[0083]
[Effect of the Invention] As mentioned above, according to this invention, in a RF device, controlling the magnitude of attenuation freely to the change sexagenary-cycle coincidence of the change of transmission and reception or two or more antennas can be realized by one semiconductor device, and the remarkable effectiveness that the formation of small lightweight and low-cost-izing of a device can be attained is acquired.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[Field of the Invention] This invention relates to the switch attenuator containing the high frequency switch and high frequency attenuator which are used for a high frequency transceiver circuit. Moreover, this invention relates to the semiconductor device which realizes this switch attenuator, and the RF device using this semiconductor device.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

PRIOR ART

[Description of the Prior Art] Drawing 1 is the block diagram showing the high frequency (referred to as "RF" below) section 10 of the transceiver circuit by the Prior art. The RF section 10 of a transceiver circuit is equipped with the RF switch 120, and, thereby, performs transmission and reception alternatively. At the time of transmission, the signal inputted in the modulating-signal input terminal (MOD in) 110 is radiated from an antenna 130 in space through a frequency converter (it considers as a "mixer" below) 112, a variable gain amplifier (it considers as "AGC amplifier" below) 114, power amplifier (PA) 116, the RF switch (RF SW) 120, and the frequency filter 122.
[0003] Conversely, at the time of reception, the signal received in the antenna 130 is outputted through the frequency filter 122, the RF switch 120, an attenuator 150, a low noise amplifier (LNA) 152, and a mixer 154 from the intermediate frequency (referred to as "IF" below) signal output terminal (IF out) 156.
[0004] transmission and reception -- in any case, a local oscillation signal with a desired frequency is generated, and a phase locked loop (referred to as "PLL" below) 170 and an oscillator 172 output it to a signal distribution box (DIV) 174. By mixing a modulating signal and a local oscillation signal, a mixer 112 generates a RF signal and outputs it to the AGC amplifier 114. By mixing a RF signal and a local oscillation signal, a mixer 154 generates an IF signal and outputs it to the IF signal output terminal 156.
[0005] Actuation of the RF section 10 of drawing 1 is explained below. The RF sections 10 are some mobile transmitters represented by the terminal of a cellular phone. In almost all cases, in a mobile transmitter, the antenna 130 (here, it thinks also including the frequency filter 122) which requires the comparatively big volume for simplification of configuration is used for the both sides of a sending circuit and a receiving circuit. In order to share the antenna section by transmission and reception, at the time of transmission, it is electrically combined with power amplifier 116, and an antenna 130 is electrically separated from a low noise amplifier 152. Conversely, at the time of reception, it dissociates from power amplifier 116 electrically, and an antenna 130 is electrically combined with a low noise amplifier 152. In order to perform the change for such transmission and reception, the semiconductor-device-ized RF switch 120 is usually adopted. The RF switch 120 by the conventional technique uses the transistor as a switching element, and it is controlling it electrically so that a transistor takes the condition of either an ON state and an OFF state.
[0006] Moreover, the terminal (for example, the hand set of a cellular phone itself) in mobile communications transmits a RF signal to a nearby base station, and communicates by receiving a RF signal from a base station. in order to maintain the power received in a base station to about 1 law, according to the distance of a terminal and a base station, it is necessary to control delicately the power transmitted from a terminal In order to maintain almost uniformly the power outputted in the IF signal output terminal 156 of a terminal on the contrary, it is necessary to control RF power inputted into a low noise amplifier 152. In order to fill these demands, generally the RF section 10 of a terminal is equipped with the AGC amplifier 114 for transmission, and the attenuator 150 for reception.
[0007] Drawing 2 is the circuit diagram of the switch 20 by the Prior art. The switch 20 is equipped with field-effect transistors (referred to as "FET" below) 200-203, the resistors 210 and 211 for impedance adjustment, the gate bias resistors 220-223, the antenna terminal 230, the transmitted power-input terminal 231, the received-power output terminal 232, the 1st control terminal 245, and the 2nd control terminal 246 in drawing 2 .
[0008] Actuation of the switch of drawing 2 is explained. At the time of transmission, by impressing a negative larger electrical potential difference than the absolute value of the threshold of FET 201 and 202 to the 2nd control terminal 246, FET 201 and 202 is made into an OFF state, and zero or a forward electrical potential difference is impressed to the 1st control terminal 245, and FET 200 and 203 is made into an ON state. Thereby, transmitted power passes along a terminal 231, FET200, and the antenna terminal 230, and is outputted to an antenna 250.
[0009] Conversely, at the time of reception, by impressing a negative larger electrical potential difference than the

absolute value of the threshold of FET 200 and 203 to the 1st control terminal 245, FET 200 and 203 is made into an OFF state, and zero or a forward electrical potential difference is impressed to the 2nd control terminal 246, and FET 201 and 202 is made into an ON state. Thereby, received power passes along an antenna 250, a terminal 230, and FET201, and is outputted to a terminal 232.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EFFECT OF THE INVENTION

[Effect of the Invention] As mentioned above, according to this invention, in a RF device, controlling the magnitude of attenuation freely to the change sexagenary-cycle coincidence of the change of transmission and reception or two or more antennas can be realized by one semiconductor device, and the remarkable effectiveness that the formation of small lightweight and low-cost-izing of a device can be attained is acquired.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] In the migration terminal equipment of a cellular phone, in order to raise portability, while lightweight[small and]-izing a device, low-cost-izing is important. In order to realize this, the miniaturization and low-cost-izing of a circuit in current and the RF section are called for strongly. However, also in which the above-mentioned conventional technique, the transceiver circuit needed to have a switch, AGC amplifier, and an attenuator separately. Consequently, it had the technical problem that the transceiver circuit by the Prior art had the size of a device, and unescapable increase of cost.
[0011] The place which it is made in order that this invention may solve the above-mentioned technical problem, and is made into the purpose is to offer the equipment which functions as small [which is used for a high frequency transceiver circuit], a light and low cost switch, and an attenuator.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

MEANS

[Means for Solving the Problem] The 1st terminal by which the switch attenuator by this invention is connected to an antenna, Have the 2nd terminal connected to a transmitter, and the 3rd terminal connected to a receiver, and are the switch attenuator which changes the 1st condition and the 2nd condition, and it sets in this 1st condition. This 1st terminal is connected to this 2nd terminal. This 1st terminal The impedance Z1 which it was intercepted from this 3rd terminal, and this 3rd terminal was connected to the ground, and was seen from this 1st terminal maintaining equal relation substantially to the impedance Z2 seen from this 2nd terminal This switch attenuator is electrically controllable and it sets in this 2nd condition so that the magnitude of attenuation between this 1st terminal and this 2nd terminal may be changed. This 1st terminal It connects with this 3rd terminal and this 1st terminal is intercepted from this 2nd terminal. This 2nd terminal So that it connects with a ground, and the magnitude of attenuation between this 1st terminal and this 3rd terminal may be changed, the impedance Z1 seen from this 1st terminal maintaining equal relation substantially to the impedance Z3 seen from this 3rd terminal This switch attenuator is electrically controllable and the above-mentioned purpose is attained by that.
[0013] With a certain operation gestalt, the 1st transistor is prepared between said 1st terminal and grounds. The 2nd transistor is prepared between said 2nd terminal and grounds. The 3rd transistor is prepared between said 3rd terminal and grounds. The 4th transistor is prepared between this 1st terminal and this 2nd terminal, the 5th transistor is prepared between this 1st terminal and this 3rd terminal, and it sets in said 1st condition. This 3rd transistor is an ON state, this 5th transistor is an OFF state, in said 2nd condition, this 3rd transistor is an ON state and this 5th transistor is an OFF state.
[0014] With a certain operation gestalt, it is contained substantially [said impedance Z1] in the range of 0.5xZA-2.0xZA, is contained substantially [said impedance Z2] in the range of 0.5xZT-2.0xZT, and is contained substantially [said impedance Z3] in the range of 0.5xZR-2.0xZR, and ZA, ZT, and ZR express the impedance of said antenna, said transmitter, and said receiver here, respectively.
[0015] With a certain operation gestalt, each of said 1st transistor, said 2nd transistor, said 3rd transistor, said 4th transistor, and said 5th transistor the dual gate field-effect transistor which has a drain, the source, and the two gates -- it is -- this -- one gate of the two gates it connects with this drain -- having -- **** -- this -- the gate of another side of the two gates is connected to this source -- having -- **** -- this -- the two gates receive the electrical potential difference for electric control through resistance, respectively.
[0016] The 1st terminal by which the switch attenuator by this invention is connected to the 1st antenna, It has the 2nd terminal connected to a transmitter, the 3rd terminal connected to a receiver, and the 4th terminal connected to the 2nd antenna. Are the switch attenuator which changes the 1st condition, the 2nd condition, the 3rd condition, and the 4th condition, and it sets in this 1st condition. It connects with this 2nd terminal, and this 1st terminal is intercepted from this 3rd terminal. This 3rd terminal Connect with a ground and this 4th terminal is intercepted from this 1st terminal, this 2nd terminal, this 3rd terminal, and this ground. The impedance Z1 seen from this 1st terminal maintaining equal relation substantially to the impedance Z2 seen from this 2nd terminal, so that the magnitude of attenuation between this 1st terminal and this 2nd terminal may be changed This switch attenuator is electrically controllable and it sets in this 2nd condition. It connects with this 3rd terminal, and this 1st terminal is intercepted from this 2nd terminal. This 2nd terminal Connect with a ground and this 4th terminal is intercepted from this 1st terminal, this 2nd terminal, this 3rd terminal, and this ground. The impedance Z1 seen from this 1st terminal maintaining equal relation substantially to the impedance Z3 seen from this 3rd terminal, so that the magnitude of attenuation between this 1st terminal and this 3rd terminal may be changed This switch attenuator is electrically controllable and it sets in this 3rd condition. It connects with this 2nd terminal, and this 4th terminal is intercepted from this 3rd terminal. This 3rd terminal Connect with a ground and this 1st terminal is intercepted from this 2nd

terminal, this 3rd terminal, this 4th terminal, and this ground. The impedance Z4 seen from this 4th terminal maintaining equal relation substantially to the impedance Z2 seen from this 2nd terminal, so that the magnitude of attenuation between this 4th terminal and this 2nd terminal may be changed This switch attenuator is electrically controllable and it sets in this 4th condition. It connects with this 3rd terminal, and this 4th terminal is intercepted from this 2nd terminal. This 2nd terminal Connect with a ground and this 1st terminal is intercepted from this 2nd terminal, this 3rd terminal, this 4th terminal, and this ground. The impedance Z4 seen from this 4th terminal maintaining equal relation substantially to the impedance Z3 seen from this 3rd terminal, so that the magnitude of attenuation between this 4th terminal and this 3rd terminal may be changed This switch attenuator is electrically controllable and the above-mentioned purpose is attained by that.

[0017] With a certain operation gestalt, the 1st transistor is prepared between said 1st terminal and grounds. The 2nd transistor is prepared between said 2nd terminal and grounds. The 3rd transistor is prepared between said 3rd terminal and grounds. The 4th transistor is prepared between this 1st terminal and this 2nd terminal. The 5th transistor It is prepared between this 1st terminal and this 3rd terminal, and the 6th transistor is prepared between said 4th terminal and grounds. The 7th transistor is prepared between this 2nd terminal and this 4th terminal, the 8th transistor is prepared between this 3rd terminal and this 4th terminal, and it sets in said 1st condition. This 3rd transistor is an ON state. This 5th transistor, this 6th transistor, this 7th transistor, and this 8th transistor It is an OFF state and sets in said 2nd condition. This 2nd transistor It is an ON state. This 4th transistor, this 6th transistor, this 7th transistor, and this 8th transistor It is an OFF state and sets in said 3rd condition. This 3rd transistor It is an ON state. This 1st transistor, this 4th transistor, this 5th transistor, and this 8th transistor It is an OFF state, and in said 4th condition, this 2nd transistor is an ON state and this 1st transistor, this 4th transistor, this 5th transistor, and this 7th transistor are OFF states.

[0018] With a certain operation gestalt, it is contained substantially [said impedances Z1 and Z4] in the range of 0.5xZA-2.0xZA, is contained substantially [said impedance Z2] in the range of 0.5xZT-2.0xZT, and is contained substantially [said impedance Z3] in the range of 0.5xZR-2.0xZR, and ZA, ZT, and ZR express the impedance of said antenna, said transmitter, and said receiver here, respectively.

[0019] With a certain operation gestalt, on the semi-conductor substrate, it integrates and is formed.

[0020] With a certain operation gestalt, it has power amplifier further, and this power amplifier is integrated and formed on said semi-conductor substrate.

[0021] With a certain operation gestalt, it has the low noise amplifier further, and this low noise amplifier is integrated and formed on said semi-conductor substrate.

[0022]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained, referring to a drawing. The same reference mark expresses the same component.

[0023] The "switch attenuator" in this specification says the equipment it has equipment and the function of RF switch for antennas, and RF attenuator so that it may mention later. Moreover, a "node" does not necessarily need the terminal for connection with the equipment exterior.

[0024] (Gestalt 1 of operation) Drawing 3 is the block diagram of the RF section 30 of the portable telephone with which the 1st operation gestalt of the switch attenuator of this invention is used. The switch attenuator 40 of this invention combines electrically an antenna 130, and power amplifier 116 or a low noise amplifier 152 according to the condition of transmission and reception. The switch attenuator 40 combines a node T1 with a node T2 electrically at the time of transmission, and, more specifically, combines node T3 with a ground electrically. Moreover, the switch attenuator 40 combines a node T1 with node T3 electrically at the time of reception, and combines a node T2 with a ground electrically. The ground in this specification is connected to the case shielded in RF while the negative electrode of a power source is connected and it offers common potential about the both sides of a direct-current (referred to as "DC" below) signal, and a RF signal. The flow of the signal at the time of the transmission and reception in the RF section 30 is the same as drawing 1 explained.

[0025] Since the switch attenuator 40 by this invention has a switch and the function of an attenuator so that it may mention later, it has the big effectiveness that the AGC amplifier 114 and attenuator 150 of drawing 1 can be lost. Moreover, if it manufactures as a semiconductor device which had the switch attenuator 40 unified, drastic reduction of size and cost is more desirable than a possible next door. In addition, all the transmission lines that connect each block of drawing 3 have the characteristic impedance of 50 ohms. Moreover, although the RF section 30 is used as some portable telephones, it is not limited to this here. The RF section 30 can be widely used for the equipment which transmits and receives a RF signal, and it can use the switch attenuator 40 widely as equipment to attenuate

while changing a RF signal.
[0026] In drawing 3 , the control voltage generator valve flow coefficient 1 is generated based on the data in which the control voltage for setting up the condition of FET contained in the switch attenuator 40 as shown in Table 1 - 4 explained later was stored by the read only memory ROM 1, and is supplied to each FET. A read only memory ROM 1 stores the data for generating the control voltage of FET corresponding to the condition of Table 1 - 4.
[0027] Drawing 4 is the circuit diagram of the 1st operation gestalt of the switch attenuator by this invention. The switch attenuator 40 is equipped with nodes T1 and T2 and T3, and is connected to an antenna 130, power amplifier 116, and a low noise amplifier 152, respectively. The control voltage generator valve flow coefficient 1 generates the electrical potential difference which controls FET based on the data stored in the read only memory ROM 1, and outputs it to nodes CT1-CT5.
[0028] FET Q1 connects a node T1 to a ground with a certain impedance. The control voltage received in the node CT 1 minds resistance R12, and is FET. It is added to the gate of Q1 and is FET. This predetermined impedance of Q1 is changed. It responds to the control voltage of a node CT 1, and, specifically, is FET. Q1 can take the impedance of the large range from an ON state to an OFF state. FET In an ON state, the impedance of Q1 is low to extent it can consider that is zero, and high to extent it can consider that is infinite in an OFF state. FET Since it is the depletion type of N type, Q1 is FET. It is FET conversely that what is necessary is just to give the electrical potential difference Vgs between the gate sources more than 0 [V] in order to make Q1 into an ON state. What is necessary is just to give the electrical potential difference Vgs between the gate sources below a threshold VTH [V] (VTH<0), in order to make Q1 into an OFF state. FET When filling the relation which the electrical potential difference Vgs between the gate sources of Q1 becomes VTH<Vgs<0, it sets on these specifications, and it is FET. Q1 is made to call that it is the "intermediate state" of an ON state and an OFF state. FET Q1 is the Schottky barrier gate mold FET (referred to as "MESFET" below) with the gestalt of this operation. As mentioned above, FET It sets on these specifications and the explanation about Q1 is FET. It is applied also about Q2-Q4.
[0029] FET It is FET like Q1. Q2 and Q3 connect a node T2 and T3 to a ground with a certain impedance, respectively. The control voltage received in nodes CT2 and CT3 minds resistance R22, and is FET, respectively. Resistance R32 is minded [of Q2] again, and it is FET. It is added to the gate of Q3 and is FET, respectively. The impedance of Q2 and Q3 is changed. Resistance R12, R22, and R32 is resistance for gate bias.
[0030] FET Between the source of Q1, Q2, and Q3, and a ground, resistance R11, R21, and R31 is formed, respectively. These resistance R11, R21, and R31 is FET, respectively. Impedance matching is taken by adjusting the nodes T1 and T2 in case Q1, Q2, and Q3 are ON states, and the impedance between T3 and a ground.
[0031] FET It is FET like Q1. Q4 and Q5 connect a node T2 and T3 to a node T1 with a certain impedance, respectively. The control voltage received in nodes CT4 and CT5 minds resistance R42, respectively, and is FET. Resistance R52 is minded [of Q4] again, and it is FET. It is added to the gate of Q5 and the impedance of FETQ4 and Q5 is changed, respectively.
[0032] Next, actuation of the switch attenuator 40 is explained. The switch attenuator 40 has the following modes of operation 1-4. Namely, transmission without mode 1:attenuation, transmission with mode 2:attenuation, the reception without mode 3:attenuation, and the mode 4: It is reception with attenuation. Attenuation between a node T1, and a node T2 or node T3 of "attenuation" is said here. For example, in the mode 1, attenuation between a node T1 and a node T2 does not exist. The mode 1 is used when the migration terminal containing the RF section 30 is distant from the base station (i.e., when supplying an antenna 130, without attenuating the RF signal outputted from power amplifier 116). The mode 2 is used when the migration terminal which contains the RF section 30 conversely is close to a base station (i.e., since the RF signal outputted from power amplifier 116 is attenuated when supplying an antenna 130). It is applied also when it is reception that it is the same as that of the case of transmission. The mode 3 is used when the migration terminal containing the RF section 30 is distant from the base station (i.e., when supplying a low noise amplifier 152, without attenuating the RF signal inputted from the antenna 130). The mode 4 is used when the migration terminal which contains the RF section 30 conversely is close to a base station (i.e., since the RF signal inputted from the antenna 130 is attenuated when supplying a low noise amplifier 152).
[0033] The switch attenuator 40 of this invention can change the magnitude of attenuation of the switch attenuator 40 continuously by changing the control voltage of a switching element (here FET) in the mode 2 and the mode 4 so that it may mention later. Consequently, the switch attenuator of this invention does big effectiveness so in the mobile communication which can take a range with large output power at the time of transmission and input power at the time of reception.
[0034] (Mode 1) FET of the switch attenuator 40 in the mode 1 The condition of Q1-Q5 is shown in Table 1.

[0035]
[Table 1]

FET	Q1	Q2	Q3	Q4	Q5
状態	オフ	オフ	オン	オン	オフ

[0036] It is FET in order to realize the mode 1 of the switch attenuator 40. What is necessary is just to impress the control voltage corresponding to each condition of setting Q1-Q5 as the condition which shows in Table 1 to nodes CT1-CT5. It is FET as mentioned above. It is FET that what is necessary is just to apply the electrical potential difference for example, more than 0 [V] to each gate in order to make Q1-Q5 into an ON state. What is necessary is just to apply the electrical potential difference for example, below VTH [V] to each gate, in order to make Q1-Q5 into an OFF state.
[0037] Drawing 5 is the representative circuit schematic of the switch attenuator 40 in the mode 1. In drawing 5 , the closed switch expresses FET of an ON state and the open switch expresses FET of an OFF state. As the mode 1 is shown in drawing 5 , an impedance is mostly connected to a node T2 by zero, as for node T3, an impedance is mostly connected to a ground by zero, and node T3 is intercepted for the node T1 from the node T1 and the node T2. Therefore, the RF signal outputted from power amplifier 116 in the mode 1 is FET, without receiving and decreasing in a node T2. An antenna 130 is supplied through Q4 and a node T1. Moreover, node T3 which is an input terminal to a low noise amplifier 152 is FET. It prevents Q's3 connecting with a ground and an unnecessary RF signal being inputted by that cause into a low noise amplifier 152.
[0038] The insertion loss of the switch attenuator 40 in the mode 1 is FET. It is only about 0.5dB resulting from the impedance (that is, impedance equivalent to on resistance) of the ON state of Q4.
[0039] (Mode 2) FET of the switch attenuator 40 in the mode 2 The condition of Q1-Q5 is shown in Table 2.
[0040]
[Table 2]

FET	Q1	Q2	Q3	Q4	Q5
状態	中間	中間	オン	中間	オフ

[0041] It is FET in order to realize the mode 2 of the switch attenuator 40. What is necessary is just to impress the control voltage corresponding to each condition of setting Q1-Q5 as the condition which shows in Table 2 to nodes CT1-CT5. In the mode 2 and the mode 4, FET is used by the intermediate state. FET What is necessary is just to apply to each gate the electrical potential difference which becomes 0<Vgs<VTH as an electrical potential difference Vgs between the gate sources, in order to make Q1-Q5 into an intermediate state.
[0042] Drawing 6 is the representative circuit schematic of the switch attenuator 40 in the mode 2. In drawing 6 , the closed switch expresses FET of an ON state, the open switch expresses FET of an OFF state, and resistance expresses FET of an intermediate state. Hereafter, the impedance of FETQ1-Q5 of an intermediate state is made to express like ZQ1-ZQ5, respectively. As the mode 2 is shown in drawing 6 , it connects with a node T2 with an impedance ZQ4, and a node T1 is connected to a ground with an impedance ZQ1. A node T2 is connected to a ground with an impedance ZQ2. As for node T3, an impedance is mostly connected to a ground by zero, and node T3 is intercepted from the node T1 and the node T2. Therefore, it is received in a node T2, it is accompanied by the desired magnitude of attenuation, and the RF signal outputted from power amplifier 116 in the mode 2 is FET. An antenna 130 is supplied through Q1, Q2, Q4, and a node T1. Moreover, node T3 which is an input terminal to a low noise amplifier 152 is FET. It prevents Q's3 connecting with a ground and an unnecessary RF signal being inputted by that cause into a low noise amplifier 152.
[0043] The magnitude of attenuation of the switch attenuator 40 in the mode 2 is FET. It changes changing the control voltage applied to the gate of Q1, Q2, and Q4, i.e., by changing impedances ZQ1, ZQ2, and ZQ4. The value of the control voltage applied to the gate of FETQ1, Q2, and Q4 is beforehand stored in the read only memory ROM 1, for example, and is read according to the required magnitude of attenuation. For example, if the control voltage generator valve flow coefficient 1 which is a programmable voltage generator generates control voltage based on the data showing the control voltage read from ROM1 and outputs to the gate of each FET, the mode 2 and the mode 4 only for a desired amount to attenuate a RF signal are realizable. Moreover, ROM1 is FET. The data showing the control voltage (that is, the electrical potential difference more than each 0 [V] and the electrical potential difference below VTH [V]) applied to the gate of Q3 and Q5 may be stored collectively. Furthermore, it sets in the modes 1, 3,

and 4, and ROM1 is FET. The data showing the control voltage applied to Q1-Q5 may be stored collectively.
[0044] (Mode 3) FET of the switch attenuator 40 in the mode 3 The condition of Q1-Q5 is shown in Table 3.
[0045]
[Table 3]

FET	Q1	Q2	Q3	Q4	Q5
状態	オフ	オン	オフ	オフ	オン

[0046] It is FET in order to realize the mode 3 of the switch attenuator 40. What is necessary is just to impress the control voltage corresponding to each condition of setting Q1-Q5 as the condition which shows in Table 3 to nodes CT1-CT5.
[0047] Drawing 7 is the representative circuit schematic of the switch attenuator 40 in the mode 3. As the mode 3 is shown in drawing 7 R> 7, an impedance is mostly connected to node T3 by zero, mostly, an impedance is connected to a ground by zero and the node T2 is intercepted [the node T2] for the node T1 from a node T1 and node T3. Therefore, the RF signal inputted from the antenna 130 in the mode 3 is FET, without receiving and decreasing in a node T1. A low noise amplifier 152 is supplied through Q5 and node T3. Moreover, the node T2 which is an output terminal from power amplifier 116 is FET. It prevents Q's2 connecting with a ground and an unnecessary RF signal being outputted by that cause to a low noise amplifier 152.
[0048] The insertion loss of the switch attenuator 40 in the mode 3 is FET. It is only about 0.5dB resulting from the impedance of the ON state of Q5.
[0049] (Mode 4) FET of the switch attenuator 40 in the mode 4 The condition of Q1-Q5 is shown in Table 4.
[0050]
[Table 4]

FET	Q1	Q2	Q3	Q4	Q5
状態	中間	オン	中間	オフ	中間

[0051] It is FET in order to realize the mode 4 of the switch attenuator 40. What is necessary is just to impress the control voltage corresponding to each condition of setting Q1-Q5 as the condition which shows in Table 4 to nodes CT1-CT5.
[0052] Drawing 8 is the representative circuit schematic of the switch attenuator 40 in the mode 4. As the mode 4 is shown in drawing 8 R> 8, it connects with node T3 with an impedance ZQ5, and a node T1 is connected to a ground with an impedance ZQ1. Node T3 is connected to a ground with an impedance ZQ3. Mostly, an impedance is connected to a ground by zero, and the node T2 is intercepted for the node T2 from a node T1 and node T3. Therefore, it is received in a node T1, it is accompanied by the desired magnitude of attenuation, and the RF signal inputted from the antenna 130 in the mode 4 is FET. A low noise amplifier 152 is supplied through Q1, Q3, Q5, and node T3. Moreover, the node T2 which is an output terminal from power amplifier 116 is FET. It prevents Q's2 connecting with a ground and an unnecessary RF signal being inputted by that cause into a low noise amplifier 152.
[0053] The magnitude of attenuation of the switch attenuator 40 in the mode 4 is FET. It changes changing the control voltage applied to the gate of Q1, Q3, and Q5, i.e., by changing impedances ZQ1, ZQ3, and ZQ5. The value of the control voltage applied to the gate of FETQ1, Q3, and Q5 is beforehand stored in the read only memory ROM 1, as explained in the mode 2, and it is read according to the required magnitude of attenuation.
[0054] The magnitude of attenuation can be changed filling the relation it is substantially unrelated ZT1=ZT2=Z0 in the mode 2 according to the gestalt of the 1st operation. An impedance ZT1 expresses the impedance of the switch attenuator 40 seen from the node T1, an impedance ZT2 expresses the impedance of the switch attenuator 40 seen from the node T2, and an impedance Z0 expresses the characteristic impedance (for example, 50ohms) of the circuit connected outside here. The magnitude of attenuation can be changed filling similarly the relation it is substantially unrelated ZT1=ZT3=Z0 in the mode 4 according to the gestalt of the 1st operation. An impedance ZT3 expresses the impedance of the switch attenuator 40 seen from node T3 here.
[0055] Moreover, even if above-mentioned ZT1=ZT2=Z0 and the relation it is unrelated ZT1=ZT3=Z0 are not filled, it is desirable that relation called 0.5xZA<=ZT1 <=2.0xZA, 0.5xZT<=ZT2 <=2.0xZT, and 0.5xZR<=ZT3 <=2.0xZR is filled. An impedance ZA expresses the characteristic impedance of the circuit (here antenna 130) connected to a node T1, an impedance ZT expresses the characteristic impedance of the circuit (here power amplifier 116) connected to a node T2, and an impedance ZR expresses the characteristic impedance of the circuit (here low noise amplifier 152)

connected to node T3 here.
[0056] Drawing 9 is the top view of the switch attenuator 40 of this invention integrated and formed on the semiconductor substrate. As shown in drawing 9 , the switch attenuator 40 is integrated and formed on the gallium-arsenide (referred to as "GaAs" below) substrate 901. "GND" of drawing 9 expresses a ground and other reference marks correspond with them in drawing 4 . FET Q1-Q5 are MESFET(s), and they are formed by ion-implantation on the GaAs substrate 901. FET Gate length is 0.5 micrometers and the gate width of the size of Q1-Q5 is 800 micrometers. The closure of the semiconductor chip which realized the switch attenuator 40 shown in drawing 9 is carried out to the resin mold package of ten pins, and it is made available.
[0057] (Gestalt 2 of operation) Drawing 10 is the circuit diagram of the 2nd operation gestalt of the switch attenuator by this invention. FET of drawing 10 Q1D, Q2D, Q3D, Q4D, and Q5D are dual gate FET. FET The gate bias resistors R13 and R14, R23 and R24, R33 and R34, R43 and R44, and R53 and R54 are connected to the 1st gate and the 2nd gate of Q1 D-Q5D, respectively. Moreover, FET Between the 2nd gate of Q1D - Q5D, and a drain, capacitors C13, C23, C33, C43, and C53 are connected, respectively, and it is FET. Between the 1st gate of Q1 D-Q5D, and the source, capacitors C14, C24, C34, C44, and C54 are connected, respectively.
[0058] As for the 2nd operation gestalt, it differs from the 1st operation gestalt that the capacitor is connected between that dual gate FET is used instead of, and a drain and the 2nd gate and between the source and the 1st gate. [a single gate FET] According to the configuration of the 2nd operation gestalt, the nonlinearity which FET has can be reduced and the outstanding distorted property can be realized.
[0059] (Gestalt 3 of operation) Drawing 11 is the block diagram of the RF section 1100 of the portable telephone with which the 3rd operation gestalt of the switch attenuator of this invention is used. The switch attenuator 1200 of this invention combines electrically antennas 130 or 131, and power amplifier 116 or a low noise amplifier 152 according to the condition of transmission and reception.
[0060] More specifically, the switch attenuator 1200 intercepts the node which one is electrically combined with a node T2 of a node T1 and the T four at the time of transmission, combines node T3 with a ground electrically, and is not combined with a node T2 among a node T1 and T four from other nodes and grounds.
[0061] Moreover, the switch attenuator 1200 intercepts the node which one is electrically combined with node T3 of a node T1 and the T four at the time of reception, combines a node T2 with a ground electrically, and is not combined with node T3 among a node T1 and T four from other nodes and grounds. Unlike having used the antenna with the 1st single operation gestalt, the 3rd operation gestalt can use two antennas 130 and 131. Therefore, in addition to the effectiveness of the 1st operation gestalt, the 3rd operation gestalt has the effectiveness that two antennas 130 and 131 can be alternatively used according to the situation of transmission and reception. The configuration of this 3rd operation gestalt enables for example, space diversity transmission and reception. In addition, all the transmission lines that connect each block of drawing 11 have the characteristic impedance of 50 ohms.
[0062] The control voltage generator valve flow coefficient 2 in drawing 11 and drawing 12 and a read only memory ROM 2 function as the control voltage generator valve flow coefficient 1 and a read only memory ROM 1 similarly except for the nodes which supply the electrical potential difference which controls FET being CT1-CT8.
[0063] Drawing 12 is the circuit diagram of the 3rd operation gestalt of the switch attenuator by this invention. In order to join together electrically of a node T2 and T3 to one, the switch attenuator 1200 adds node T four to the component of the switch attenuator 40, and is FET. It has further Q6-Q8, the resistance R62, R72, and R82 for gate bias, nodes CT6-CT8, and the resistance R61 for impedance matching.
[0064] Next, actuation of the switch attenuator 1200 is explained. The switch attenuator 1200 has the following modes of operation 1-8. Namely, the transmission without attenuation using the mode 1:antenna 130, the mode 2 : The transmission with attenuation using an antenna 130, Mode 3 : The reception without attenuation using an antenna 130, the reception with attenuation using the mode 4:antenna 130, mode 5: -- they are the transmission without attenuation using an antenna 131, the transmission with attenuation using the mode 6:antenna 131, the reception without attenuation using the mode 7:antenna 131, and reception with attenuation using the mode 8:antenna 131. The modes 1-4 of the 3rd operation gestalt are equivalent to the mode 1 of the 1st operation gestalt - the mode 4, respectively. Node T four of the modes 5-8 of the 3rd operation gestalt is the same as that of the modes 1-4 except for being electrically combined with a node T2 or T3 instead of a node T1.
[0065] What is necessary is just to impress the control voltage corresponding to each condition of setting FETQ1-Q8 as the condition which shows in following Table 5 - 12, respectively to nodes CT1-CT8, in order to realize the modes 1-8 of the switch attenuator 1200. The representative circuit schematic in the mode 1 of the switch

attenuator 1200 - the mode 8 is shown in drawing 13 - drawing 20 , respectively.

[0066]

[Table 5]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オフ	オン	オン	オフ	オフ	オフ	オフ

[0067]

[Table 6]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	中間	中間	オン	中間	オフ	オフ	オフ	オフ

[0068]

[Table 7]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オン	オフ	オフ	オン	オフ	オフ	オフ

[0069]

[Table 8]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	中間	オン	中間	オフ	中間	オフ	オフ	オフ

[0070]

[Table 9]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オフ	オン	オフ	オフ	オフ	オン	オフ

[0071]

[Table 10]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	中間	オン	オフ	オフ	中間	中間	オフ

[0072]

[Table 11]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オン	オフ	オフ	オフ	オフ	オフ	オン

[0073]

[Table 12]

FET	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
状態	オフ	オン	中間	オフ	オフ	中間	オフ	中間

[0074] With the gestalt of the 3rd operation, the magnitude of attenuation can be changed like the gestalt of the 1st operation, filling substantially ZT1=ZT2=Z0 and the relation it is unrelated ZT1=ZT3=Z0 in the modes 2 and 4, respectively. Moreover, with the gestalt of the 3rd operation, the magnitude of attenuation can be changed in the modes 6 and 8, filling substantially ZT4=ZT2=Z0 and the relation it is unrelated ZT4=ZT3=Z0, respectively. An impedance ZT4 expresses the impedance of the switch attenuator 1200 seen from node T four here.

[0075] Moreover, even if the above-mentioned ZT1=ZT2=Z0, ZT1=ZT3=Z0, ZT4=ZT2=Z0, and the relation it is unrelated ZT4=ZT3=Z0 are not filled, it is desirable that relation called 0.5xZA<=ZT1 <=2.0xZA, 0.5xZT<=ZT2 <=2.0xZT, 0.5xZR<=ZT3 <=2.0xZR, and 0.5xZB<=ZT4 <=2.0xZB is filled. An impedance ZB expresses the characteristic impedance of the circuit (here antenna 131) connected to node T four here.

[0076] With the gestalt of the 1st explained above - the 3rd operation, by setting FET as the middle condition of ON

and OFF, also when the property of the circuit connected to a switch attenuator changes, it can respond flexibly. Such property change of the circuit connected may take place, when changing the power outputted from the power amplifier for transmission.

[0077] Although a desired characteristic impedance is obtained with the gestalt of the above-mentioned implementation in the frequency band used, for example by the communication link between a portable telephone and a base station, it is not limited to this frequency band, but can apply to RF band widely.

[0078] Based on the indication of the gestalt of the 2nd operation, the further effectiveness that the outstanding distorted property is realizable can also be acquired by transposing FET of the gestalt of the 3rd operation to dual gate FET.

[0079] FET used for the switch attenuator of this invention is not limited to a depletion type, but an enhancement type may be used for it. Moreover, FET should just be the device which is not limited to this although it is MESFET, but can control an impedance by the above-mentioned operation gestalt electrically with the control terminal. As long as conditions, such as an operating frequency and parasitic capacitance of a device proper, allow, a PIN diode, the PN-junction mold FET, a MOSFET, etc. may be used, for example.

[0080] Moreover, if the switch attenuator by this invention is integrated and formed on a semi-conductor substrate with power amplifier or a low noise amplifier, reduction of size and cost can be aimed at and it is more desirable.

[0081] The control voltage generators valve flow coefficient1 and valve flow coefficient2 and read only memories ROM1 and ROM2 will not be restricted to the configuration explained with the gestalt of the above-mentioned implementation, if the control voltage for setting the condition of FET of the switch attenuator by this invention as the condition of either an ON state, an intermediate state and an OFF state can be generated. For example, a programmable voltage generator without the memory which stores data in digital one may be used. Moreover, random access memory may be used instead of read only memories ROM1 and ROM2.

[0082] As shown in Table 2, Table 4, Table 6, and Table 8, 10, and 12, with the gestalt of above-mentioned operation, three FET is set as an intermediate state at the time of the transmission with attenuation, or reception. However, the number of FET of an intermediate state is not restricted to three pieces, but when at least one FET is an intermediate state, the desired magnitude of attenuation should just be obtained.

[Translation done.]

* NOTICES *

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram of the radio-frequency head 10 of the transceiver circuit by the Prior art.
[Drawing 2] It is the circuit diagram of the switch 20 by the Prior art.
[Drawing 3] It is the block diagram of the RF section 30 of the portable telephone with which the 1st operation gestalt of the switch attenuator of this invention is used.
[Drawing 4] It is the circuit diagram of the 1st operation gestalt of the switch attenuator by this invention.
[Drawing 5] It is the representative circuit schematic of the switch attenuator 40 in the mode 1.
[Drawing 6] It is the representative circuit schematic of the switch attenuator 40 in the mode 2.
[Drawing 7] It is the representative circuit schematic of the switch attenuator 40 in the mode 3.
[Drawing 8] It is the representative circuit schematic of the switch attenuator 40 in the mode 4.
[Drawing 9] It is the top view of the switch attenuator 40 of this invention integrated and formed on the semi-conductor substrate.
[Drawing 10] It is the circuit diagram of the 2nd operation gestalt of the switch attenuator by this invention.
[Drawing 11] It is the block diagram of the RF section 1100 of the portable telephone with which the 3rd operation gestalt of the switch attenuator of this invention is used.
[Drawing 12] It is the circuit diagram of the 3rd operation gestalt of the switch attenuator by this invention.
[Drawing 13] It is the representative circuit schematic of the switch attenuator 1200 in the mode 1.
[Drawing 14] It is the representative circuit schematic of the switch attenuator 1200 in the mode 2.
[Drawing 15] It is the representative circuit schematic of the switch attenuator 1200 in the mode 3.
[Drawing 16] It is the representative circuit schematic of the switch attenuator 1200 in the mode 4.
[Drawing 17] It is the representative circuit schematic of the switch attenuator 1200 in the mode 5.
[Drawing 18] It is the representative circuit schematic of the switch attenuator 1200 in the mode 6.
[Drawing 19] It is the representative circuit schematic of the switch attenuator 1200 in the mode 7.
[Drawing 20] It is the representative circuit schematic of the switch attenuator 1200 in the mode 8.
[Description of Notations]
40 Switch Attenuator
Q1, Q2, Q3, Q4, Q5 FET
R11, R12, R21, R22, R31, R32, R42, R52 Resistance
T1, T2, T3, CT1, CT2, CT3, CT4, CT5 Node
130 Antenna

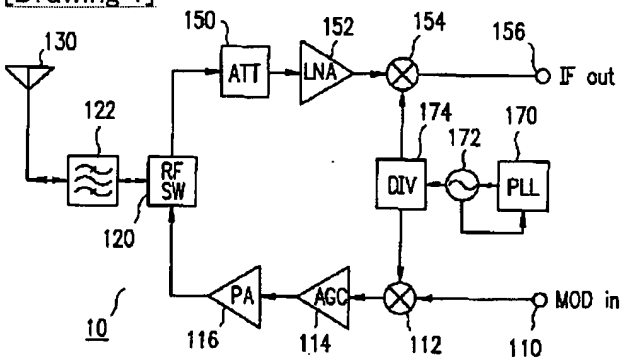
[Translation done.]

* NOTICES *

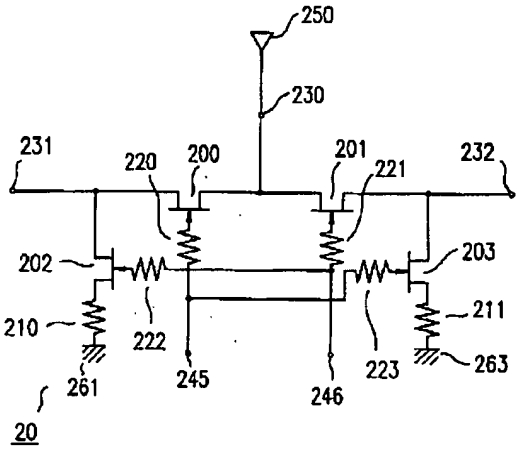
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

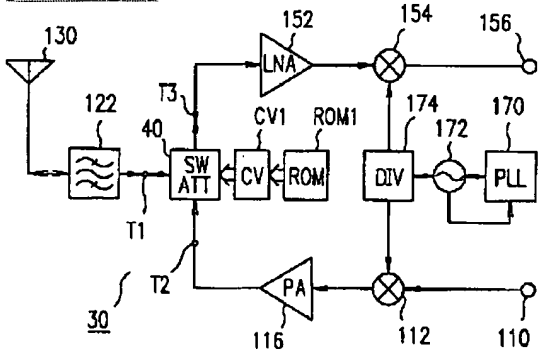
[Drawing 1]



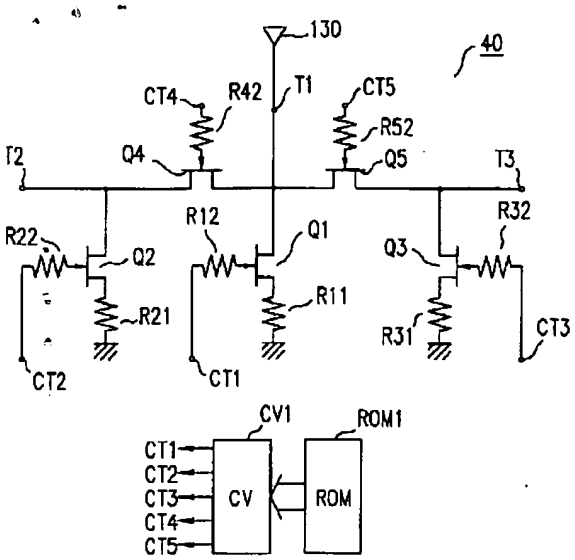
[Drawing 2]



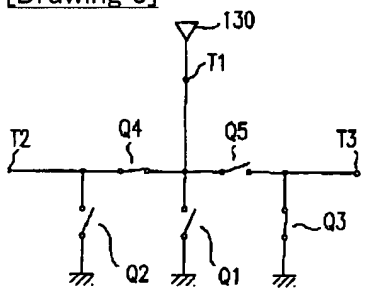
[Drawing 3]



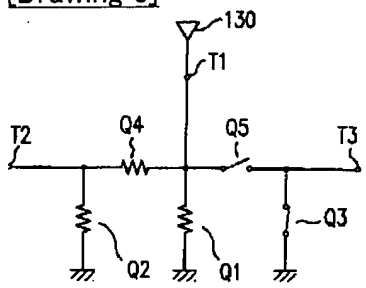
[Drawing 4]



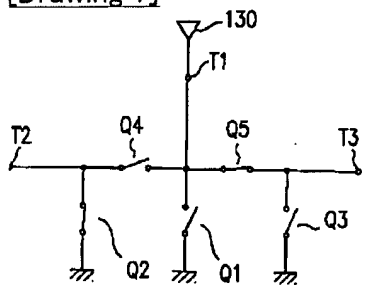
[Drawing 5]



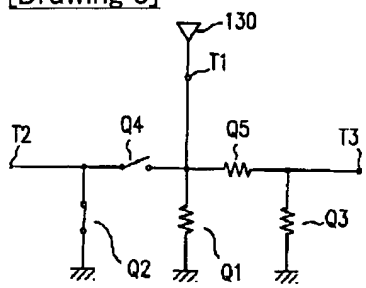
[Drawing 6]



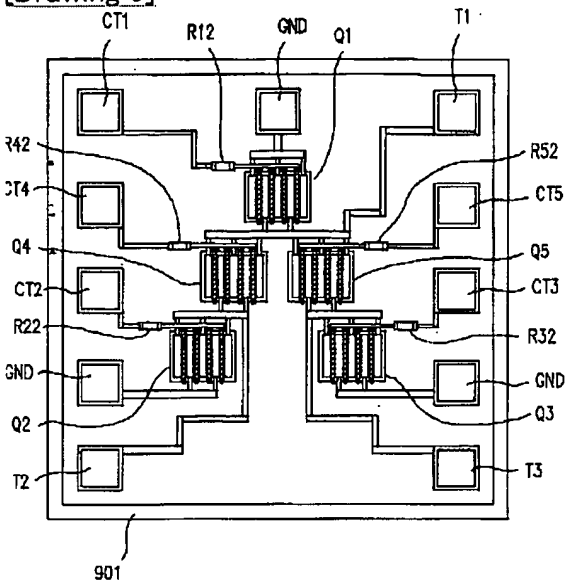
[Drawing 7]



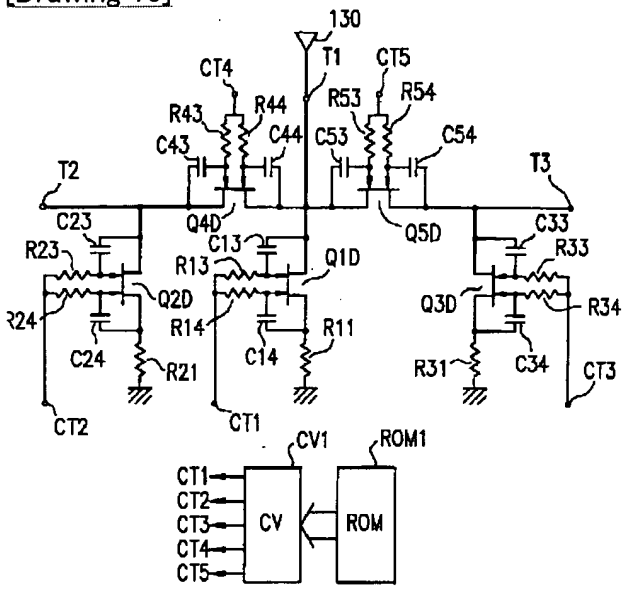
[Drawing 8]



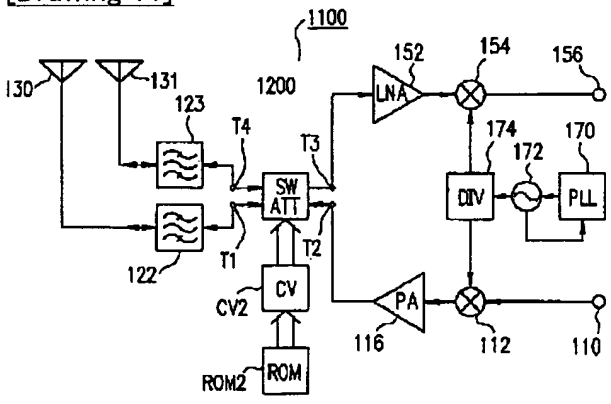
[Drawing 9]



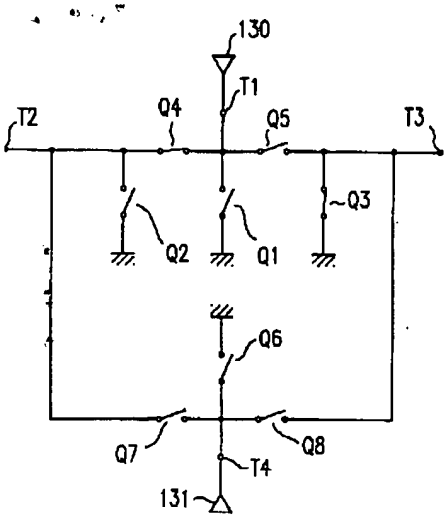
[Drawing 10]



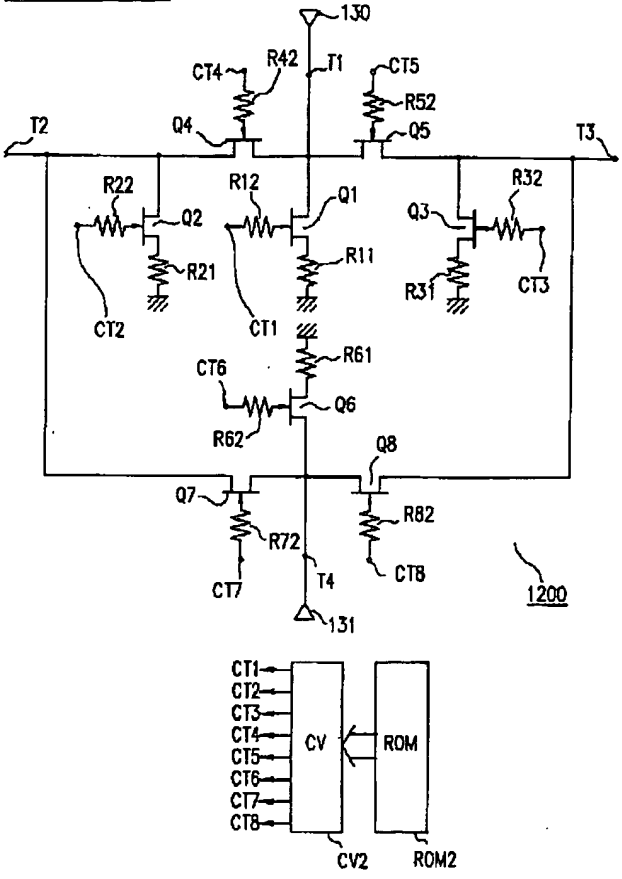
[Drawing 11]



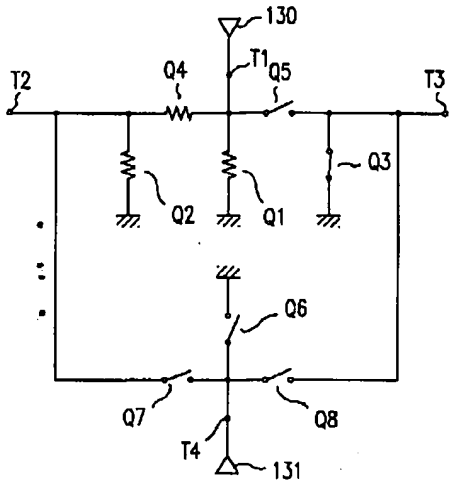
[Drawing 13]



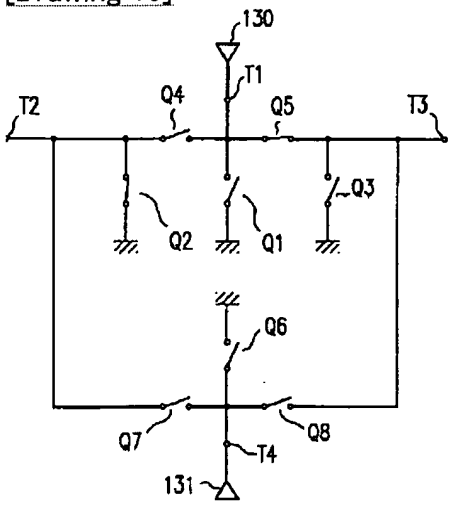
[Drawing 12]



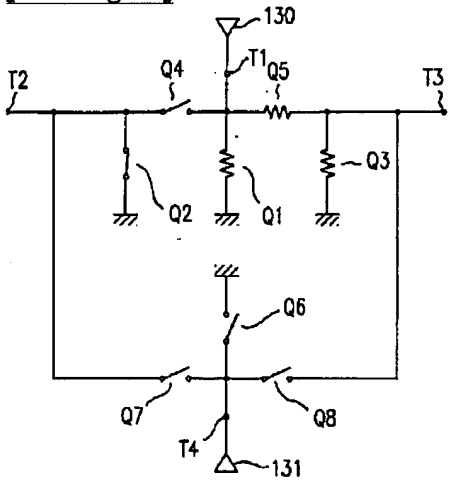
[Drawing 14]



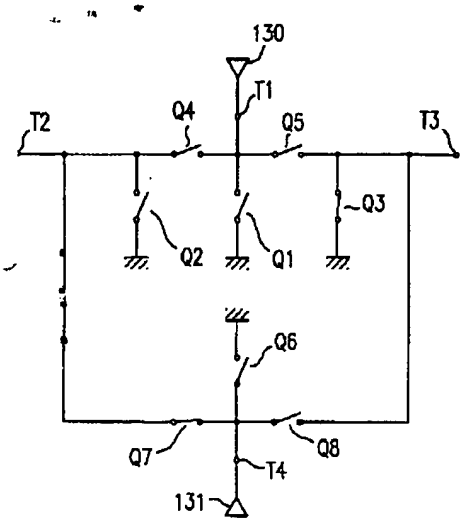
[Drawing 15]



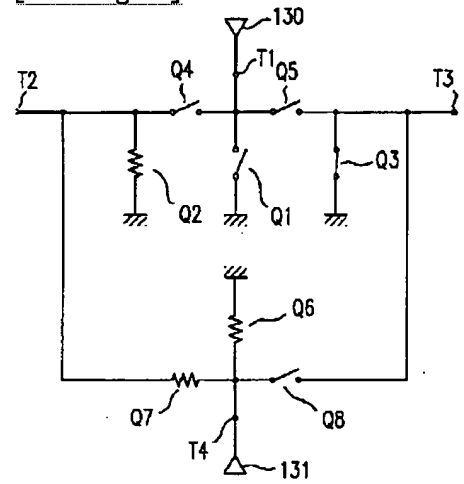
[Drawing 16]



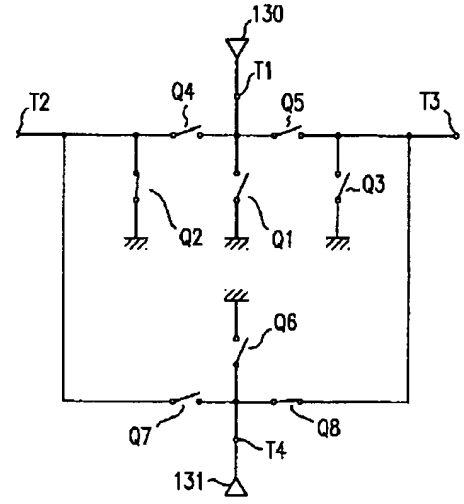
[Drawing 17]



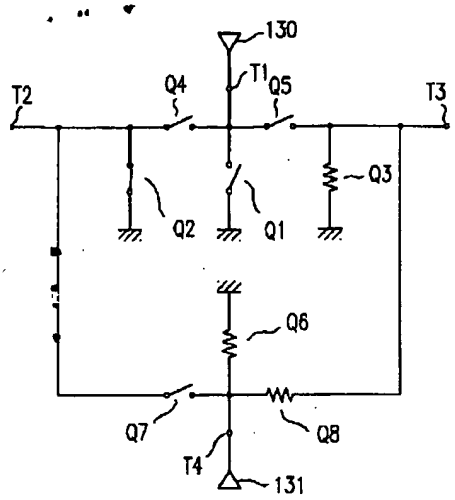
[Drawing 18]



[Drawing 19]



[Drawing 20]



[Translation done.]